Unit-IV
ADVANCED INTEL PROCESSORS

80286 microprocessor:

The 80286 microprocessor is a third generation,16-bit microprocessor. It is the advanced version of the 8086 processor and is designed for multiuser and multitasking environments. The 80286 performance is six times faster than the 8086 microprocessor.

Features:

- ✓ The intel 80286 is a high performance **16-bit microprocessor** designed for **multitasking and multi programming.**
- ✓ The 80286 can be operated at **three** different clock speeds. These are **12.5MHz, 10MHz, 8MHz.**
- ✓ It has 24-bit address bus so it can directly address **16M bytes** of physical memory.
- ✓ It has **1G bytes** of virtual (not physical) memory.
- ✓ It is housed in a **68 pin leadless flat package**.
- ✓ It is operated in two modes they are **real address mode** and **protected virtual address mode (**PVAM).
- ✓ It has four functional units they are **bus unit** (BU), **address unit** (AU), **instruction unit(**IU), and **execution unit**(EU).
- ✓ It has four general purpose registers of size 16-bit and they are **AX**,**BX**,**CX**,**DX** and four special purpose registers of size 16-bit and they are **IP,SP**,**BP**,**SI**,**DI**.
- ✓ It has four segment registers of size 16-bit and they are **CS**, **DS, ES,** and **SS**.
- ✓ It has a 16 bit flag register in that **15 flags** are used. They are **AF** (auxiliary carry flag),**CF** (carry flag),**ZF** (zero flag),**OF** (overflow flag),**SF** (sign flag),**TF** (trap flag),**IF** (interrupt flag),**DF** (direction flag), similar to 8086. The additional 6 flags are **IOPL** (i/o privilege field),**NT** (nested task),**PE** (protection enable),**MP** (monitor processor extension),**EM** (processor extension emulator), and **TS** (task switch).
- ✓ Through **memory management unit** the 80286 addresses a virtual memory space of 1G bytes.
- ✓ The 80286 performance is **six times** faster than the 8086 microprocessor.

Block diagram of 80286:

The architecture of 80286 is divided into four functional units. They are bus unit, address unit, instruction unit, and execution unit. The block diagram is given below figure. The function of each block is explained below

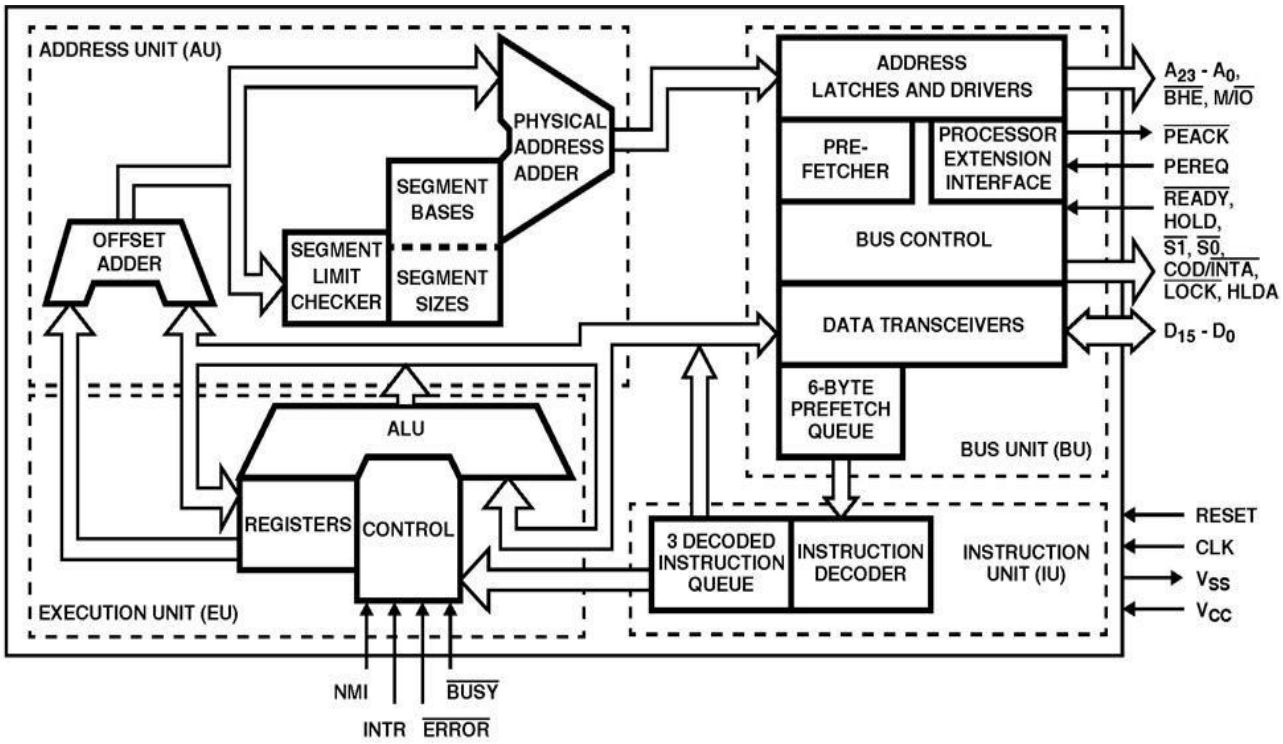
Address unit (AU):

- The address unit is responsible for calculating the 20-bit physical address of instructions and data that the CPU wants to access it.
- This unit calculates the 20-bit physical address based on the contents of the 16-bit segment register and a 16-bit offset value. And the 80286 addresses a 1M byte of physical memory as same as 8086 in **real address mode**.
- In protected virtual address mode, the AU operates as a **memory management unit** (MMU) and utilizes all 24 address lines to provide 16M bytes of physical memory.
- In PVAM mode the physical address is calculated by using the selector, data descriptor table, and data descriptor.

Bus unit (BU): The bus unit main purpose is to provide the communication between the 80286 microprocessor with the outside of the world(peripheral devices). The functions of bus unit is given below

- The physical address computed by the AU is handed over the bus unit (BU).

- The BU fetches the instructions, reads data from memory and I/O ports and write data to memory and I/O ports.



- This BU involves the concept of **"*instruction pipelining*"** which fetches the instructions from the memory and stored them in 6-byte prefetch instruction queue.
- The BU also contains the processor extension interface block which is used to connect the math processors (80287) to the 80286.
- The data transceivers interface and control the internal data bus with the system bus.

Instruction unit(IU): The instruction unit receives the prefetched instructions from 6-byte prefetch instruction queue of the bus unit(BU) and decode it. The functions of IU is given below

- The instruction decoder in the IU is used to decode the instructions from the 6-byte prefetch instruction queue and is given to the 3-decoded instruction queue.
- The 3-decoded instruction queue is used to store the decoded instructions from the instruction decoder.

Execution unit(EU): The execution unit takes the decoded instructions from the IU and execute them. The functions of EU is given below

- The EU has a 16-bit ALU which performs the arithmetic and logical operations.
- It has 4 general purpose registers for handling the data and 4 special purpose registers for offset address calculation.
- It has a control unit which generates the necessary control signals for the system operations.

80386 microprocessor:

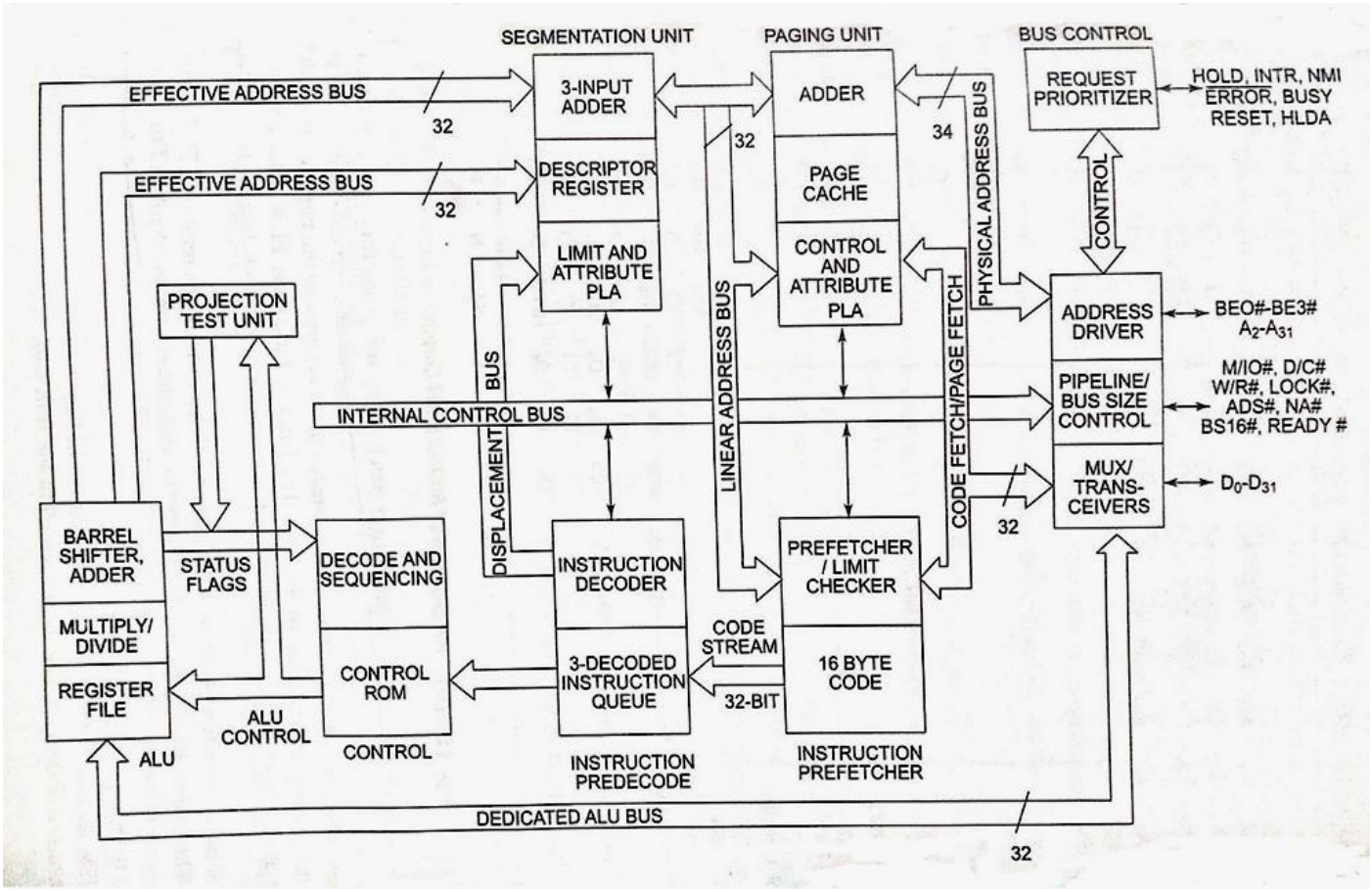
Features of 80386:

- ✓ It is a 32-bit microprocessor.
- ✓ It has 32-bit data bus.
- ✓ It has 32-bit address bus.
- ✓ It can access 2^{32} = 4 GB physical memory.
- ✓ It can access 64TB virtual memory.
- ✓ It is upward compatible with 8086 instruction set.

- ✓ It has **on-chip address translation cache**.
- ✓ The memory management unit of 80386 can support the concept of **paging**, used to organize the segmented memory into pages. Each page is of 4KB size.
- ✓ The 80386 can be supported by 80387 for mathematical data processing.
- ✓ 80386 are available in 132-pin grid array package and have 20MHz and 33MHz versions.
- ✓ In 80386 memory management unit provides **four level protection mechanism** for protecting and isolating the system code and data from application program.
- ✓ The 80386 can run 8086 applications under protected mode in its virtual 8086 mode of operation.
- ✓ It has four general purpose registers of size 32-bit and they are **EAX**, **EBX**, **ECX**, **EDX** and four special purpose registers of size 32-bit and they are **EIP,ESP**,**EBP,ESI,EDI**.
- ✓ It has four segment registers of size 16-bit and they are **CS**, **DS, ES, SS,FS,GS**.
- ✓ It has a 32 bit flag register-**EFLAGS**

Architecture of 80386:

The architecture of 80386 is divided into three sections, they are central processing unit, memory management unit and bus control unit.



Central processing unit:

The central processing unit is further divided into execution unit and instruction unit.

- The execution unit has eight general purpose and eight special function registers, they are used to store data operands and offset addresses.
- The instruction unit decodes the opcode bytes received from the 16-byte code queue and the decoded instructions are stored in 3-decoded instruction queue.
- The decoded instructions then passed to the control section for deriving the necessary control signals.
- The barrel shifter is used to increase the speed of the shift and rotate operations.
- The multiply/divide logic implements bit-shift-rotate algorithms to complete the operations (arithmetic operations like division and multiplication) in minimum time.

Memory management unit:

The memory management unit consists of segmentation and paging unit.

- The segmentation unit allows two address components. They are segment address and offset address for sharing of code and data.
- The segmentation allows maximum size of 4GB segments.
- The paging unit organizes the physical and virtual memory in terms of pages of size 4KB.
- The paging unit works under the control of segmentation unit.
- Each segment is further divided into pages of size 4KB.
- The segmentation unit provides four level protection mechanism for protecting and isolating system code from application program.

Bus control unit:

Bus control unit is used to control the system bus in allocating bus to various external devices.

- The bus control unit has a prioritiser to resolve the priority of various bus requests, to control the access of the bus.
- The address driver drives the bus enable and address lines A0-A31.
- The pipeline and dynamic bus sizing units handle the related control signals like M/IO#, D/C#, W/R#, LOCK# etc.
- The data buffers interfaces the internal data bus with the system bus.

80486 microprocessor:

Features of 80486:

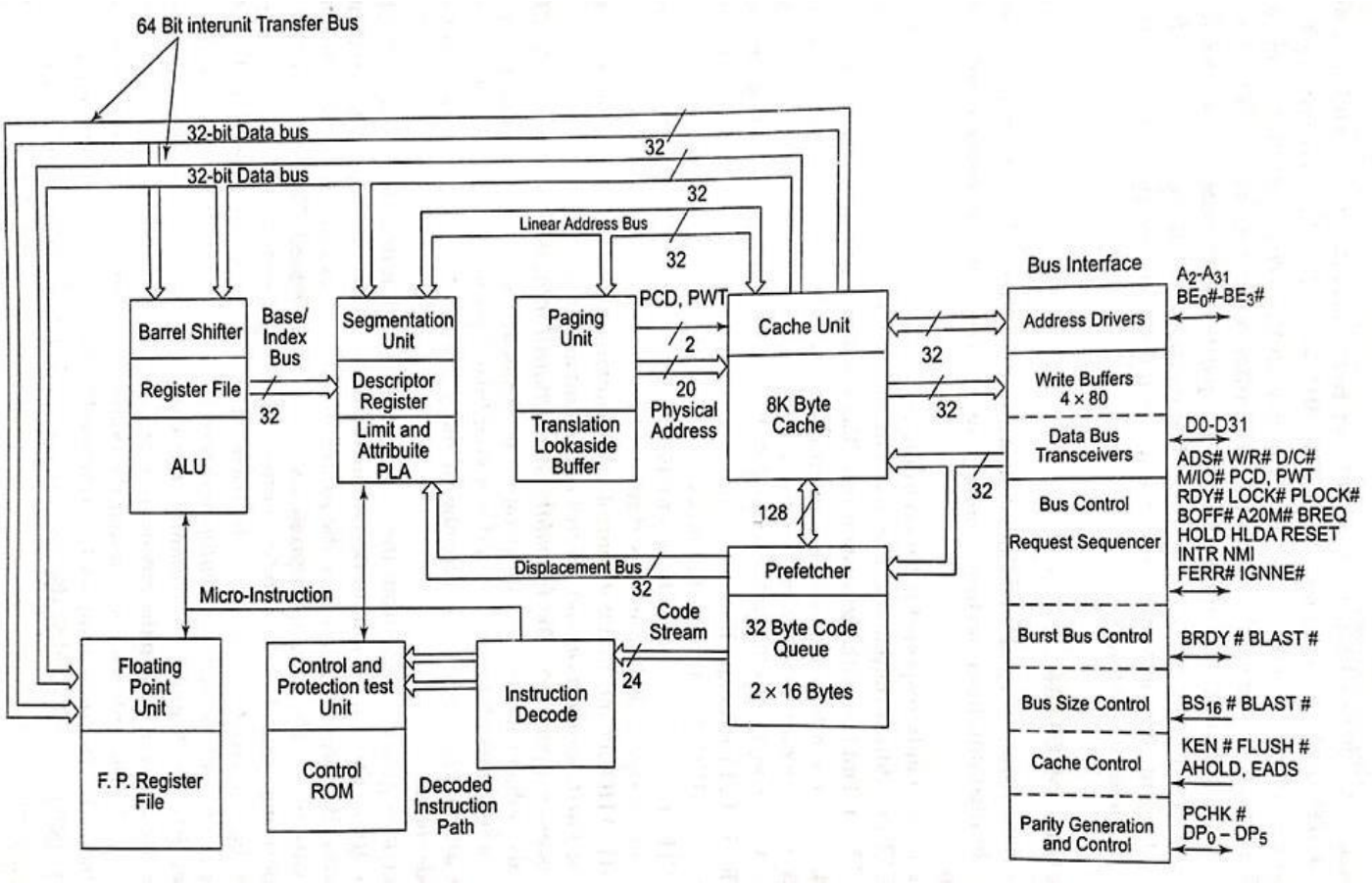
- ✓ 80486 is a 32-bit microprocessor.
- ✓ 80486 is 168 pin ic available in pin grid array package.
- ✓ 80486 is available in different versions with different clock frequencies, i.e., 25MHz, 33MHz, 50 MHz and 100MHz.
- ✓ It has 32-bit data bus.
- ✓ 32-bit address bus.
- ✓ It can access the 4GB physical memory.
- ✓ It can access 64TB virtual memory.
- ✓ It is the first CPU with on chip Floating point unit (FPU).
- ✓ For fast execution of complex instructions 80486 has introduced 5 stage pipeline.
- ✓ It has 8KB on chip cache, used to store programs and data.
- ✓ It has boundary scan test feature.
- ✓ On-line parity checking also introduced in 80486.

Architecture of 80486:

The internal architecture of 80486 is broadly divided into three sections, namely bus interface unit, execution and control unit and floating point unit.

Bus interface unit:

- The bus interface unit is responsible for coordinating all the bus operations.
- The address driver interfaces the internal address bus output of cache unit with the system bus.
- The data bus transceivers interface the internal 32-bit data bus with the system bus.
- The 4 X 80 write data buffer is used to hold the 80-bit data to be written to the memory.
- The bus control and request sequencer handles the signals like ADS#, W/R#, D/C#, M/IO#, HOLD and HLDA etc.
- The burst control signals BRDY# and BLAST# are used during burst cycle.
- The cache control signals KEN#, FLUSH, AHOLD and EADS# used to control and maintain the cache.



- The bus size control signals BS_{16}# and BS_8 are used for dynamic bus sizing.
- Parity generation and control unit is used to generate the parity and to detect the errors.
- Boundary scan control unit is used to perform boundary scan tests to ensure the correct functioning of the hardware components.

Execution and control unit:

The execution and control unit is used to fetch the instruction, decode the instructions and generate the control signals for execution of the instructions.

- The prefetcher fetches the codes from memory ahead of execution time and arranges them in 32-byte code queue.
- The instruction decoder fetches the code from the 32-byte queue and decodes it sequentially. The decoded instructions are given to the control unit.
- The control ROM stores the microprogram for deriving the control signals for execution of different instructions.
- The ALU and register bank is used for execution.
- The segmentation unit, descriptor registers, paging unit, translation look aside buffer and limit and attribute PLA work together to manage virtual memory.

Floating point unit:

The 80486 has on-chip floating point unit used to perform floating point mathematical operations. The floating point unit has floating point registers to perform mathematical operations.

- The floating point unit with register bank communicates with the bus interface unit under the control of memory management unit via its 64-bit internal data bus.
- The floating point unit is responsible for carrying out mathematical data processing at a higher speed compared to ALU, with its built in floating point algorithms.

Compare/contrast the features of 80286, 80386, 80486 processors

Parameter	80286	80386	80486
CPU clock speed	12.5MHz, 10MHz and 8MHz versions	20,25 and 33MHz clock versions	33MHz, 50MHz
No of pins	68-pin IC available in leadless flat package	132-pin IC available in Pin Grid Array (PGA) package.	168-pin IC available in Pin Grid Array (PGA) package.
Processor size	16- bit	32-bit	32-bit
Data bus size	16-bit	32-bit	32-bit
Address bus size	24-bit	32-bit	32-bit
Physical address accessing capability	16MB	4GB	4GB
Virtual memory addressing capability	1GB	64TB	64TB
Features	• In built Memory Management unit (MMU) • supports multitasking	• four levels of code protection • supports paging • address translation cache • supports paging	• 5 stage pipelining • On chip 8KB cache • On chip math coprocessor unit (Floating point unit) • Boundary scan • Parity check
Operating modes	• Real addressing mode • Protected virtual addressing mode	• Protected virtual address mode • Real address mode • Virtual 8086 mode	• Protected virtual address mode • Real address mode • Virtual 8086 mode
Cache	no	Address translation cache	8KB data and code cache
compatibility	Compatible with previous microprocessors	Compatible with previous microprocessors	Compatible with previous microprocessors

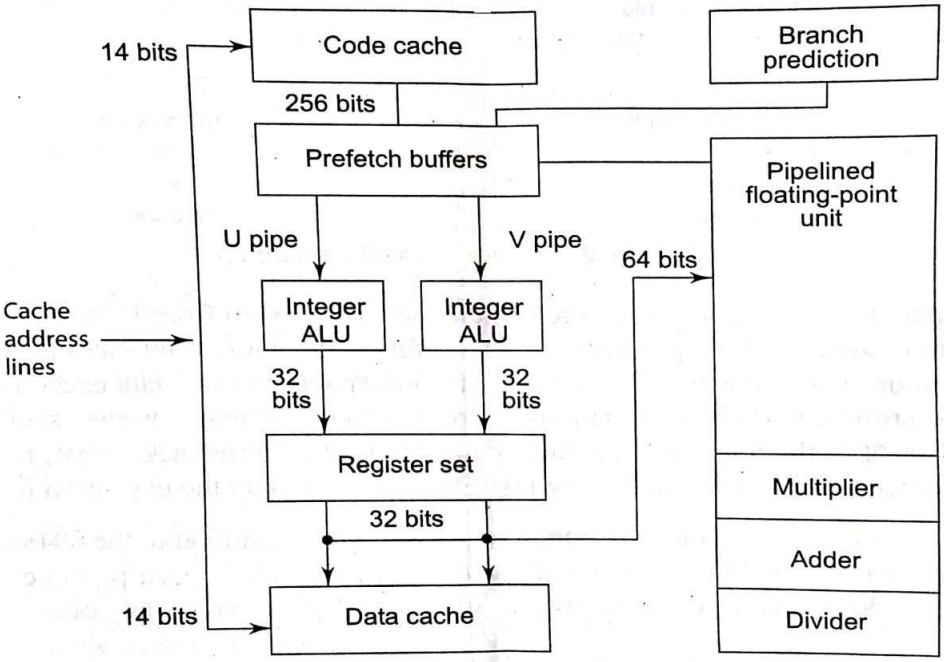
80586 (PENTIUM) processor: Pentium is a 32-bit microprocessor introduced in 1993. It a 296 pin ic available in standard pin grid array (SPGA) package.

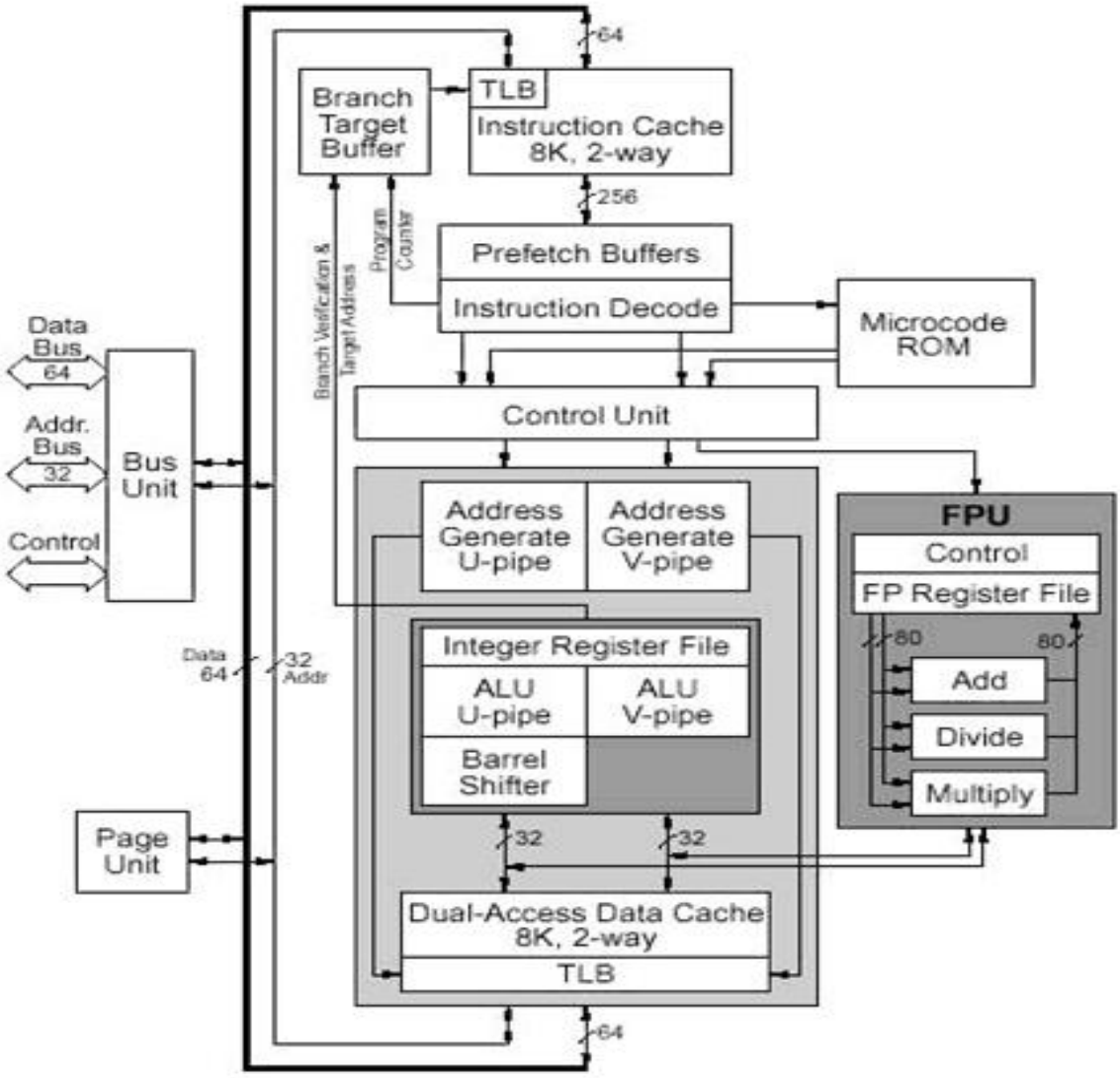
Features of 80586 (PENTIUM):

- ✓ Super scalar and super pipelined architecture.
- ✓ Pipelined floating point unit.
- ✓ Separate code and data caches.
- ✓ 64-bit data bus.
- ✓ 32-bit address bus.
- ✓ It can access 4GB of physical memory and 64TB of virtual memory.
- ✓ Pipelined bus cycles.
- ✓ Address parity.
- ✓ Internal parity checking.
- ✓ Branch prediction.
- ✓ Performance monitoring.
- ✓ Dual processing support.

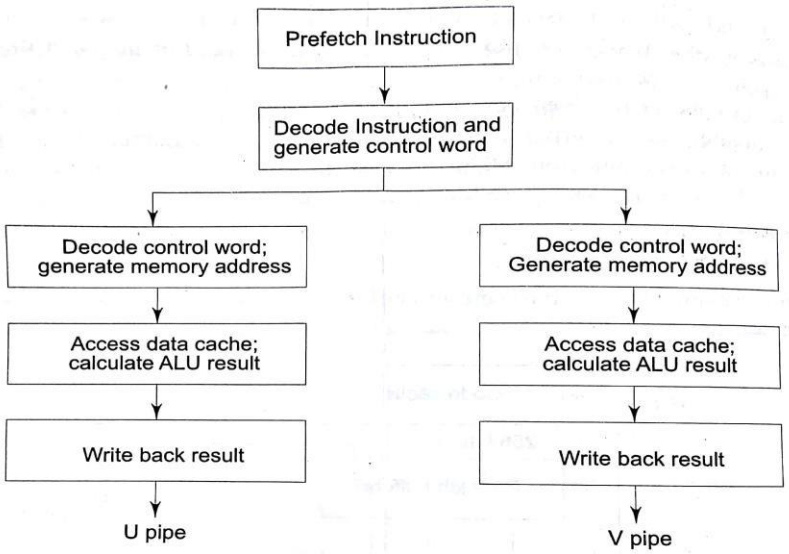
Explain the Architecture of Pentium microprocessor ,80586 Architecture:

Super scalar Organisation: The architecture of pentium processor is given below figure.





- ✓ The Pentium processor has super scalar architecture which **allows parallel execution of two instructions**.
- ✓ For execution of multiple instructions concurrently, Pentium issues two instructions in parallel to the two independent integer pipelines known as U and V pipelines. Each of these are five stage pipelines.
- ✓ The super scalar architecture is explained by using the below figure.
- ✓ From the above figure the first stage is prefetch stage. In this stage, the instructions are prefetched from the code cache and stored in the prefetch buffer.



- ✓ Decoding stage '1' is used to decode the simple instructions and generate the control words.
- ✓ The output of decoding stage '1' is given to the decoding stage '2'.
- ✓ The decode stage '2' is furtherly decodes the control words and generate memory address.
- ✓ By using the memory address from the D2 stage, the data is accessed from the data cache and given to the ALU.
- ✓ Last stage in pipelining is Write back stage. In this stage the processor updates the registers contents based on the executed result.

Separate code cache and Data cache:

- ✓ The 80586 has separate 8KB code and Data cache memories. The 8KB code cache memory is used to store the code or instructions.
- ✓ The 8KB data cache memory is used to store the data.

Floating point unit (FPU):

- ✓ The Pentium has 8 stage pipelined floating point unit, hence the speed of the pentium is higher than the speed of 80486.
- ✓ FPU is used to perform the floating point operations. The floating point unit consists of the following blocks.
  - Floating-point multiplier segment (FAND), which is used to perform the floating point multiplication.
  - Floating-point adder segment (FADD), which is used to perform the floating point addition.
  - Floating-point Divider segment (FDD), which is used to perform the floating point division.
  - Floating-point Exponent segment (FEXP), which is used to calculate the floating point exponent.
  - Floating-point Rounder segment (FRD), which is used rounded off the floating point addition and division result before write back to the floating point registers.

Branch Prediction: In this scheme, a prediction is made for the branch instruction currently in the pipeline. The prediction will either be taken or not taken. If the prediction is true then the pipeline will not be flushed and no clock cycles will be lost. If the prediction is false then the pipeline is flushed and starts over with the current instruction

Features of advanced Pentium processors:

Pentium Pro: Pentium pro was introduced in 1995 and consists of 5.5 million transistors. It is a 387 pin IC and available in pin grid array (PGA) package.

Features of Pentium pro:

- ✓ It is a 32-bit super scalar CISC processor.
- ✓ It has 64-bit data bus and 36-bit address bus.
- ✓ It can able to access 64GB of physical memory.
- ✓ Five parallel execution units and 12-stage super pipeline.
- ✓ Dynamic execution
  - Out of order execution.
  - Speculative execution.
- ✓ DIB (Dual individual bus) architecture.
- ✓ Register renaming.
- ✓ Error checking and correcting codes.
- ✓ Scalable up to four processors.
- ✓ Integrated level two (L2) cache of 256KB/512KB/1MB.
- ✓ The clock frequencies of Pentium pro are 150MHz/166MHz/180Mhz200MHz.

Pentium II: the Pentium II is released in the year 1997 and consists of 7.5 million transistors. It is actually Pentium pro processor with on chip MMX (Multi Media Extension).

Features of Pentium II:

- ✓ It is a 32-bit microprocessor.
- ✓ It has 64-bit data bus and 36-bit address bus.
- ✓ It cn able to access 64GB of physical memory and 64TB of virtual memory.
- ✓ It supports dynamic execution.
- ✓ Integrated primary (L1) 16kb instruction cache and 16kb data cache.
- ✓ It has integrated 256kb secondary (L2) cache.
- ✓ Fully compatible with previous versions.
- ✓ Supports MMX technology.
- ✓ Integrated thermal diode for measuring processor temperature.

Pentium III: the pentium III processor was introduced in the year 1999 which contains 9.5 million transistors. The higher clock version of pentium III consists of 23 million transistors. It is 370 pin IC available in pin grid array (PGA) package.

Features of Pentium III:

- ✓ It is a 32-bit microprocessor.
- ✓ It has 64-bit data bus and 36-bit address bus.
- ✓ It cn able to access 64GB of physical memory and 64TB of virtual memory.
- ✓ It has dynamic execution microarchitecture.
- ✓ Fully compatible with previous microprocessors.
- ✓ Integrated level one 16kb instruction cache and 16kb data cache.
- ✓ Integrated 512kb level two cache.
- ✓ Error correcting code for system bus data.
- ✓ It operates with clock frequency range 500MHz to 1GHz.
- ✓ Intel processor serial number.
- ✓ Internet streaming SIMD (Single instruction and Multiple Data) extensions for enhanced video, sound and 3D performance.

Pentium 4: The pentium 4 was released in the year 2000 and consists of 42 million transistors. The pentium 4 processor with hyper threading was released in the year 2002 and consists of 53 million transistors.

Features of Pentium 4:

- ✓ It is based on NetBurst microarchitecture.
- ✓ It has 42 million transistors.
- ✓ Hyper Threading technology was introduced in Pentium 4.
- ✓ It has Hyper pipelined technology.
- ✓ Clock speeds varies from 1.4GHz to 1.7GHz.
- ✓ Pentium 4 NetBurst architecture introduces internet Streaming SIMD Extensions 2 (SSE2).
- ✓ It supports 400MHz system bus,Advanced dynamic execution.
- ✓ In addition to L1 8KB data cache, it also includes an execution trace cache that stores upto 12k decoded micro-ops (micro-operations). It has on-chip 256KB L2 cache.

Compare the features of advanced Pentium processors

Parameter	Pentium pro	Pentium II	Pentium III	Pentium 4
processor	32-bit	32-bit	32-bit	32-bit
Released year	1995	1997	1999	2000
No of transistors	5.5 million transistors	7.5 million transistors	9.5 million transistors	42 million transistors
No of pins	387 pin IC available in pin grid array package	242 pin IC available in single edge contact (SEC) cartridge package.	370 pin IC in PGA package	478 pin IC in PGA package
Clock speed	150/166/180/200MHz	233MHz to 450MHz	500MHz to 1GHz	1.4GHz to 2.8GHz
Features	• 12 stage pipelining • Register renaming • DIB (Dual independent Bus) architecture • Out of order execution and speculative execution.	• Quick start and deep sleep mode provides extremely low power dissipation • Supports MMX technology • Integrated thermal diode for measuring processor temperature.	• Dynamic execution microarchitecture • Error correcting code for system bus data • Internet streaming SIMD extensions (SSE) for enhanced video, sound and 3D performance • Intel processor serial number	• Intel NetBurst architecture. • Hyper threading • Hyper pipelining • Advanced dynamic execution • 144 Streaming SIMD Extension2 instructions are added.
Level one (L1) cache	8KB code cache and 8KB data cache	16KB code cache and 16KB data cache	16KB code cache and 16KB data cache	8KB data cache
Level two (L2) cache	256kb/512kb/1Mb	256KB	512KB	256KB
Execution Trace cache	no	no	no	yes