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C14–CM–303/C14–IT–303

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BOARD DIPLOMA EXAMINATION, (C–14)

MARCH/APRIL—2016

DCME—THIRD SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time : 3 hours] [*Total Marks* : 80

PART—A 3×10=30

Instructions : (1) Answer **all** questions.

(2) Each question carries **three** marks.

(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. Write about EX-OR gate. 3

2. State DeMorgan's theorems. 1½×2=3

3. Draw the full-adder diagram using two half-adders and OR gate. 3

4. Define the following terms : 1×3=3

(a) Fan-in

(b) Fan-out

(c) Noise margin

5. Define flip-flop. 3

6. Distinguish between edge triggering and level triggering. 1×3=3

7. Draw 4-bit ring counter. 3

8. List different types of data transfer in registers. 3

9. Distinguish between EEPROM and UVPROM. 3

10. List any three applications of encoders. 3

PART—B 10×5=50

Instructions : (1) Answer *any* **five** questions.

(2) Each question carries **ten** marks.

(3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. *(a)* Explain NAND and NOR gates in detail. 2½+2½=5

(b) Write the Boolean expression for Y in the following forms from the given table : 2½+2½=5

(i) Sum of products form

(ii) Product of sums form

A	*B*	*C*	*Y*
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

12. *(a)* Explain the working of serial adder. 5

(b) Simplify the following expression using K-Map : 5

$Y \quad m(0,1,2,3,5,7,8,9,10,11,13,14,15)$

13. Draw and explain RS latch using NAND gate and NOR gate. 5+5=10

14. Draw and explain the working of edge-triggered JK flip-flop with its truth table and waveforms. 4+4+2=10

15. Draw and explain 4-bit synchronous counter. 4+6=10

16. *(a)* Draw and explain the operation of a mod-8 ripple counter. 5

(b) Explain the operation of a 1 to 4 demultiplexer with neat diagram. 5

17. Explain the working of Universal Shift Register. 10

18. *(a)* Differentiate between static RAM and dynamic RAM. 5

(b) Explain the use of shift register as memory. 5

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