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BOARD DIPLOMA EXAMINATION, (C–14)

SEPTEMBER/OCTOBER - 2020

DEEE—FIFTH SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time : 3 hours] [*Total Marks* : 80

PART—A 3×10=30

Instructions : (1) Answer **all** questions.

(2) Each question carries **three** marks.

(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. Convert the binary number 10110_2 to decimal number.

2. Draw the symbol of EX-OR gate and its truth table.

3. List the characteristics of Digital IC's.

4. Define fan-in and fan-out.

5. Define the terms 'power dissipation' and 'propagation delay'.

6. Compare the performance of serial and parallel adder.

7. Realize half-adder using NAND gates.

8. What is race around condition?

9. State the necessity of clock signal.

10. List any three differences between static RAM and dynamic RAM.

PART—B

10×5=50

Instructions : (1) Answer *any* **five** questions.

(2) Each question carries **ten** marks.

(3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. Explain the basic logic gates AND, OR and NOT gates and realize them by using NAND gates.

12. Draw and explain TTL NAND gate with open collector.

13. *(a)* Compare TTL, CMOS and ECL logic families. 6

(b) List any four IC numbers of two input digital IC logic gates. 4

14. Draw and explain the operation of 1 to 4 demultiplexer.

15. *(a)* Draw the full-adder circuit and explain its operation with truth table. 7

(b) Realize a half-adder using only NOR gates. 3

16. Draw and explain asynchronous 3 bit up-down counter.

17. Explain the level clocked *D* and *T flip-flops* with the help of truth table and circuit diagram.

18. *(a)* Draw and explain the working of basic dynamic MOS RAM cell. 7

(b) Explain the working principle of NV RAM. 3

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