



C14-EE-505

4640

BOARD DIPLOMA EXAMINATION, (C-14)

OCT/NOV—2018

DEEE—FIFTH SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time : 3 hours ]

[ Total Marks : 80

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PART—A

3×10=30

**Instructions** : (1) Answer **all** questions.

(2) Each question carries **three** marks.

(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. State De Morgan's theorems.

2. Convert the following hexadecimal numbers into binary :

(a)  $3B8C_{16}$

(b)  $CAFE_{16}$

(c)  $9742_{16}$

3. Define noise margin.

4. Classify digital logic families.

5. Define the terms power dissipation and propagation delay.

6. Draw full-adder using two half adders and one OR-gate.

7. List any three applications of multiplexers.

8. Draw the symbol of edge triggered D flip-flop.

- \* 9. Define modulus of a counter.
10. Differentiate between ROM and RAM

**PART—B**

10×5=50

**Instructions :** (1) Answer *any five* questions.

(2) Each question carries **ten** marks.

(3) The answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. (a) Draw the symbols and truth tables for the following logic gates :

(i) AND

(ii) NAND

(iii) NOR

(iv) EXOR

(v) NOT

(b) Using K-Map method simplify the following Boolean function and realize using basic gates :

$$Y = \overline{A}\overline{B}\overline{C} + \overline{A}BC + A\overline{B}\overline{C} + ABC$$

12. (a) Compare among TTL, CMOS and ECL logic families.

(b) List any four IC numbers of two input digital IC logic gates.

13. Explain the working of CMOS NAND gate with a circuit diagram.

14. Realize half adder using NAND gates and NOR gates only.

15. Draw and explain  $3 \times 8$  decoder.

16. Draw and explain 4-bit asynchronous counter and draw its timing diagram.

17. Draw and explain clocked SR flip-flop using NAND gates with its truth table.

18. (a) Draw and explain the working of 4-bit shift-left register.

(b) Explain the working principle of NV RAM.

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