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C14–EE–505

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BOARD DIPLOMA EXAMINATION, (C–14)

MARCH/APRIL—2018

DEEE—FIFTH SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time : 3 hours] [*Total Marks* : 80

PART—A 3×10=30

Instructions : (1) Answer **all** questions.

(2) Each question carries **three** marks.

(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. Compare the weighted and unweighted codes.

2. Convert $(54.B)_{16}$ into decimal and binary notations.

3. Classify digital logic families.

4. List any three IC numbers of two-input digital IC logic gates.

5. Draw the open collector TTL NAND gate.

6. Draw the logic circuit of half-adder.

7. State the need of tri-state buffer.

8. List any three applications of flip-flop.

9. Draw the *T* flip-flop, using JK flip-flop.

10. Compare static RAM and dynamic RAM.

PART—B

10×5=50

Instructions : (1) Answer *any* **five** questions.

(2) Each question carries **ten** marks.

(3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. *(a)* Explain the working of universal logic gates using truth table. 6

(b) Explain the importance of parity bit. 4

12. Explain any five characteristics of digital ICs. 10

13. Draw the circuit of CMOS NAND gate and explain its operation. 10

14. Draw BCD to decimal decoder and explain its operation. 10

15. Draw and explain 4-bit parallel adder using full adders. 10

16. Draw level clocked JK flip-flop using SR flip-flop and explain with truth table. 10

17. *(a)* Compare synchronous and asynchronous counters. 4

(b) Explain how race-around condition can be avoided in Master-Slave JK flip-flop. 6

18. *(a)* Draw and explain the working of basic dynamic MOS RAM cell. 6

(b) Distinguish between EEPROM and UVPROM. 4

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