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C20-EC–105

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BOARD DIPLOMA EXAMINATION, (C-20)

JUNE/JULY—2022

DECE - FIRST YEAR EXAMINATION

ELECTRONIC COMPONENTS AND POWER SUPPLIES

Time : 3 hours] [*Total Marks* : 80

PART—A 3×10=30

Instructions : (1) Answer **all** questions.

(2) Each question carries **three** marks.

(3) Answers should be brief and straight to the point and shall not exceed five simple sentences.

1. Compare wire wound and carbon potentiometer in any three aspects.

2. Find the colour code for the resistance of 3·7 MΩ with 10% tolerance.

3. List the different switches according to mechanism of operation.

4. Classify the PCBs based on number of layers.

5. Sketch the energy level diagrams for conductor, semiconductor and insulator materials.

6. Distinguish between the drift current and diffusion current.

7. Sketch the VI-characteristics of PN diode.

8. Define beta and gamma of a transistor and give the relation between them.

9. List the advantages of JFET over BJT.

10. Explain the need for a filter in power supplies.

PART—B

Instructions : (1) Answer **all** questions.

(2) Each question carries **eight** marks.

(3) Answers should be comprehensive and criterion for valuation is the content but not the length of the answer.

11. *(a)* Explain the colour coding in resistors with an example. 8

(OR)

(b) With neat sketch describe the working of Rheostat and give it's applications. 8

12. *(a)* *(i)* Draw the ISI Symbols of SPST, SPDT, DPST and DPDT switches. 4

(ii) Define etching and list the etchants used in practice. 4

(OR)

(b) *(i)* Define MCB and mention its uses. 4

(ii) List the steps involved in preparation of PCB. 4

13. *(a)* *(i)* Explain the formation of N-type semiconductor with a neat diagram. 4

(ii) List the applications of Zenor diode. 4

(OR)

(b) *(i)* Define valance band, conduction band and forbidden energy gap. 4

(ii) Differentiate between Zenor breakdown and avalanche breakdown. 4

14. *(a)* Explain the working of *n*-channel JFET with a neat diagram. 8

(OR)

(b) Draw and explain the drain characteristics of JFET. 8

15. *(a)* Explain the working of centre tapped full wave rectifier with a neat circuit. 8

(OR)

(b) Explain the working of transistor series voltage regulator with neat a circuit. 8

PART—C

Instructions : (1) Answer the following question.

(2) Question carries **ten** marks.

(3) Answers should be comprehensive and criterion for valuation is the content but not the length of the answer.

16. *(a)* Derive the relation between I_{CBO} and I_{CEO} in terms of α and also in terms of β. 7

(b) Find the value of I_{CBO} if $\beta = 50$ and $I_{CBO} = 5\ \mu A$. 3

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