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C16-EC-**403**

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BOARD DIPLOMA EXAMINATION, (C-16)

MARCH / APRIL — 2021

DECE — FOURTH SEMESTER EXAMINATION

MICROPROCESSORS

Time : Three Hours] [*Maximum Marks* : 80

PART-A 3×10=30

Instructions : (*i*) Answer **all** questions.

(*ii*) Each question carries **three** marks.

(*iii*) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. List the features of 8085 microprocessor.

2. Define Fetch cycle, Execution cycle and Instruction cycle.

3. State the need of Memory segmentation.

4. List different General purpose registers.

5. State the meaning of :

(*a*) MUL CH

(*b*) ROL [DI],1

6. State the various addressing modes of 8086.

7. Define a 'procedure' and sate its general form in the program.

8. State the need of Subroutine.

9. List the features of 80286 microprocessor.

10. What is Super Scalar Architecture ?

PART-B

10×5=50

Instructions : (*i*) Answer any **five** questions.

(*ii*) Each question carries **ten** marks.

(*iii*) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. Draw and explain the timing diagram of an Instruction 'STA'.

12. Draw and explain the functional block diagram of 8086.

13. Explain the Interrupt Response in 8086.

14. Explain the following instructions :

(*a*) DAA

(*b*) XLAT

(*c*) LOCK

(*d*) HLT

15. Explain CALL and RET instructions.

16. Write a program to add two 32-bit numbers. The first 32-bit number is stored in the locations 9100H, 9101H, 9102H and 9103H. The second number is stored in the locations 9104H, 9105H, 9106H and 9107H. Store the result in the locations 9108H, 9109H, 910A and 910BH.

17. Explain Instruction level parallelism.

18. Compare among 80286, 386, 486 and Pentium processors.

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