# 6234

## **BOARD DIPLOMA EXAMINATIONS**

#### SEPTEMBER/OCTOBER - 2020

## **DECE – THIRD SEMESTER**

## DIGITAL ELECTRONICS

#### Time: 3 hours

Max. Marks: 80

r. P.

#### PART – A

10 X 3= 30M

- Instructions: 1. Answer all questions.
  - 2. Each question carries three marks.
  - 3. Answer should be brief and straight to the point and shall not exceed five simple sentences.
- 1. State De-Morgan's theorems.
- 2. Convert the following binary numbers into hexadecimal numbers.i) 1011011 ii)100.1101 iii)11001001.111
- Write 2' complement number for the following binary numbers.
   i)10001 ii)11111
- 4. Classify different logic families.
- 5. Draw full adder circuit using two half adders and an OR gate.
- 6. Mention any three applications of multiplexers.
- 7. List any three applications of Flip-flops.
- 8. Distinguish between synchronous and asynchronous counters.
- 9. Draw clocked RS flip-flop using NAND gates.
- 10. Classify shift registers based on data i/o.

PART – B	$5 \ge 10 = 50$
<ul> <li>ons: 1. Answer any Five questions</li> <li>2. Each question carries TEN Marks.</li> <li>3. Answer should be comprehensive and Criteria for Vais the content but not the length of the answer.</li> </ul>	aluation
Realize AND, OR, NOT operations using NAND, NOR gates.	105%
Minimize the following expression using Karnaugh map tech	nique and
realize the result with logic gates.	£**
$Y = A\overline{B}C + \overline{A}\overline{B}C + \overline{A}\overline{B}\overline{C} + A\overline{B}\overline{C} + \overline{A}BC$	10
Explain the working of CMOS NAND gate with circuit diagram.	10
Explain 4bit parallel adder cum 2's complement subtractor	
circuit with diagram.	10
Explain the working of 3x8 decoder circuit with diagram.	10
a) Explain level clocked JK Flip-flop with truth table.	7
b) What is race around condition, how to avoid it.	3
Draw and explain the working of 4-bit asynchronous counter w	vith timing
diagram.	10
a) Explain the working of diode ROM.	6
b) Compare static RAM and dynamic RAM.	4
i	<ul> <li>I Answer any Five questions</li> <li>Each question carries TEN Marks.</li> <li>Answer should be comprehensive and Criteria for Vais the content but not the length of the answer.</li> </ul> Realize AND, OR, NOT operations using NAND, NOR gates. Minimize the following expression using Karnaugh map tech realize the result with logic gates. Y=ABC+ABC+ABC+ABC Explain the working of CMOS NAND gate with circuit diagram. Explain 4bit parallel adder cum 2's complement subtractor circuit with diagram. Explain the working of 3x8 decoder circuit with diagram. a) Explain level clocked JK Flip-flop with truth table. b) What is race around condition, how to avoid it. Draw and explain the working of 4-bit asynchronous counter w diagram. a) Explain the working of diode ROM. b) Compare static RAM and dynamic RAM.

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