C14–EC–606

4740

BOARD DIPLOMA EXAMINATION, (C–14)

SEPTEMBER/OCTOBER - 2020

DECE—SIXTH SEMESTER EXAMINATION

DIGITAL CIRCUIT DESIGN THROUGH VERILOG HDL

Time : 3 hours] [*Total Marks* : 80

PART—A 3×10=30

Instructions : (1) Answer **all** questions.

(2) Each question carries **three** marks.

(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. Give the different types of CMOS fabrication process.

2. Define functional simulation.

3. Define the stick diagram.

4. Define operand and keyword.

5. Compare verilog HDL and VHDL in any three aspects.

6. Write shortly about 'real' data type.

7. Write the syntax of AND gate instantiation and also write its truth table.

8. List the delays in gate level modeling.

9. Write gate level modeling for 1-bit comparator.

10. Write verilog HDL code for *T*-flip-flop in dataflow modeling.

PART—B

10×5=50

Instructions **:** (1) Answer *any* **five** questions.

(2) Each question carries **ten** marks.

(3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. Explain about layout design rules.

12. Explain the following operators :

(a) Arithmetic operators

(b) Logical operators

(c) Reduction operators

(d) Conditional operators

(e) Concatenation and replication operators

13. *(a)* Explain port connection rules in module instantiation. 5

(b) Explain about system tasks and compiler directives. 5

14. Explain about looping statements.

15. Explain about hierarchical modeling concept with 4-bit ripple carry adder.

16. Write verilog code for *J-K* flip-flop with synchronous clock and reset.

17. Write verilog code for 8 to 3 encoder in behavioral modeling using case statement.

18. Define test bench. Write verilog code for test bench of synchronous counter.

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