

4740

BOARD DIPLOMA EXAMINATION, (C-14)

MARCH/APRIL-2019

DECE - SIXTH SEMESTER EXAMINATION

DIGITAL CIRCUIT DESIGN THROUGH VERILOG HDL

Time: 3 Hours]

[Max. Marks:80

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PART - A

10x3=30M

**Instructions :** 1) Answer **all** questions. Each question carries Three marks  
2) Answers should be brief and straight to the point and shall not exceed five simple sentences.

- 1) List the merits of CMOS technology.
- 2) Write briefly about stick diagrams.
- 3) List the steps involved in the design flow for the VLSI IC design.
- 4) Identify the components of a Verilog module definition.
- 5) Define expressions, operators and operands.
- 6) Compare Verilog HDL and VHDL.
- 7) Write about Implicit & continuous alignment delay in data flow modelling.
- 8) List the advantages of hierarchical modelling.
- 9) Write Verilog code for 2 bit comparator in behavioral modelling.
- 10) Write Verilog code for 4 to 1 multiplexer using data flow modelling.

**PART - B**

**5X10=50M**

- Instructions:** 1) Answer any **five** questions.  
2) Each question carries **ten** marks.  
3) The answer should be comprehensive and the criteria for valuation is content but not the length of the answer.

- 11) Explain CMOS fabrication process with neat diagrams.
- 12) Explain four levels of abstraction to represent the internals of a module
- 13) Explain about the data types arrays, memories and strings with an examples for each data type.
- 14) (a) Explain about the initial and always statements.  
(b) Write verilog code for Half Adder in data flow modelling.
- 15) (a) Explain the instantiations of below gates,  
i) AND gate            ii) BUF gates  
(b) Write truth tables for AND gate & BUF gate
- 16) Using Verilog code, design SISO shift register in behavior modelling.
- 17) Compare RTL and Structural level modelling.
- 18) (a) Define test bench module or stimulus module.  
(b) Explain the need of stimulus module.

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