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C14–EC–606

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BOARD DIPLOMA EXAMINATION, (C–14)

OCT/NOV—2017

DECE—SIXTH SEMESTER EXAMINATION

DIGITAL CIRCUIT DESIGN THROUGH VERILOG HDL

Time : 3 hours] [*Total Marks* : 80

PART—A 3×10=30

Instructions : (1) Answer **all** questions.

(2) Each question carries **three** marks.

(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. List the merits of CMOS technology.

2. Draw the stick diagram for CMOS inverter.

3. Write a short note on timing simulation.

4. Write the importance of HDL in VLSI design.

5. Write the components of a verilog module definition.

6. List the data types in verilog HDL.

7. Write truth table for butif1 and notif1 gates.

8. Write a short note on initial and always statement.

9. Write short notes on combinational logic and sequential circuit.

10. Write a program for D flip-flop using verilog HDL.

PART—B

10×5=50

Instructions : (1) Answer *any* **five** questions.

(2) Each question carries **ten** marks.

(3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. Explain the process of NMOS transistor fabrication with diagrams. 10

12. Explain the four levels of abstraction used in verilog HDL. 10

13. Explain the operators in verilog HDL with examples. 10

14. Explain blocking and non-blocking procedural assignments with examples. 10

15. Design full-adder using behavioural, data flow and structural modeling. 10

16. Design and write a program for 3 to 8 decoder using verilog HDL. 10

17. *(a)* Compare between RTL level and structural level modeling. 5

(b) Design and write a program for SISO shift register. 5

18. Compare among PLA, PAL, CPLD and FPGA devices. 10

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