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C14–EC–606

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BOARD DIPLOMA EXAMINATION, (C–14)

MARCH/APRIL—2017

DECE—SIXTH SEMESTER EXAMINATION

DIGITAL CIRCUIT DESIGN THROUGH VERILOG HDL

Time : 3 hours] [*Total Marks* : 80

PART—A 3×10=30

Instructions : (1) Answer **all** questions.
(2) Each question carries **three** marks.
(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. Draw the symbol of CMOS inverter.

2. Draw the stick diagram for NMOS and PMOS transistors.

3. Write a short note on timing simulation.

4. Define module in verilog HDL.

5. Define operand and keyword.

6. Write a short note on arithmetic operators.

7. Write rules for user-define primitives.

8. List the delays used in gate level design.

9. Design JK flip-flop using verilog HDL.

10. Write the applications of PLA.

PART—B

10×5=50

Instructions : (1) Answer *any* **five** questions.

(2) Each question carries **ten** marks.

(3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. Explain *n*-well process of CMOS fabrication with diagrams.

12. *(a)* Compare between verilog HDL and VHDL. 5

(b) Explain the steps involved in design flow for the VLSI IC design. 5

13. Explain all types of operators used in verilog HDL.

14. Explain hierarchical modeling.

15. Design half-subtractor using behavioral, dataflow and structural modeling.

16. Design and write a program for 3 to 3 decoder using verilog HDL.

17. *(a)* Design and write a program for PIPO shift register. 5

(b) Design and write a program for *D* flip-flop. 5

18. Design and write a program for mealy state machine using verilog HDL.

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