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C09–EC–305

3237

BOARD DIPLOMA EXAMINATION, (C–09)

OCT/NOV—2016

DECE—THIRD SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time : 3 hours] [*Total Marks* : 80

PART—A 3×10=30

Instructions : (1) Answer **all** questions.

(2) Each question carries **three** marks.

(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. Convert the following hex numbers into decimal :

(a) $2B8_{16}$

(b) $1C_{16}$

(c) $3CA_{16}$

2. Draw the symbols of NAND, NOR and Ex-OR gates.

3. List different digital logic families.

4. Realize a half-adder circuit using NOR gates only.

5. Draw the logic circuit of 3 8 decoder.

6. Draw a level clocked *T* flip-flop.

7. Draw a four-bit shift left register.

8. State the need for preset and clear inputs in flip-flops.

9. Draw the circuit of A/D converter using counter method.

10. Write any three differences between ROM and RAM.

PART—B

10×5=50

Instructions : (1) Answer *any* **five** questions.

(2) Each question carries **ten** marks.

(3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. *(a)* Use Karnaugh map to simplify the following boolean expression : 5

$$Y \quad \overline{A}\,\overline{B}\,\overline{C} \quad A\,\overline{B}\,\overline{C} \quad \overline{A}\,B\,\overline{C} \quad A\,B\,\overline{C}$$

(b) Write boolen expressions of product of max. terms from the following truth table : 5

Inputs			*Output*
A	*B*	*C*	*X*
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

12. *(a)* Subtract decimal number 45 from 87 using 2's complement method. 4

(b) Compare between weighted and unweighted codes. 3

(c) Explain the use of parity bit. 3

13. Draw and explain 2's compliment parallel adder/subtractor circuit with one example. 10

14. *(a)* Draw and explain a simple tristate buffer. 5

(b) Draw and explain one-bit digital comparator. 5

15. *(a)* Draw and explain the operation of NAND latch. 5

(b) Write about level triggering and edge triggering. 5

16. Draw and explain master-slave JK flip-flop. 10

17. *(a)* Explain the terms resolution, accuracy and monotonicity of D/A converter. 5

(b) Draw *R*-2*R* ladder network D/A converter. 5

18. *(a)* Explain the working of dynamic MOS RAM cell. 5

(b) Compare static RAM with dynamic RAM in any five aspects. 5

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