* 3 2 3 7 *

C09–EC–305

3237

BOARD DIPLOMA EXAMINATION, (C–09)

MARCH/APRIL—2014

DECE—THIRD SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time : 3 hours] [*Total Marks* : 80

PART—A 3×10=30

Instructions : (1) Answer **all** questions.
(2) Each question carries **three** marks.
(3) Answer should be brief and straight to the point and shall not exceed *five* simple sentences.

1. Convert the following binary numbers into hexa decimal :
(a) 10100010_2
(b) 1110011_2
(c) 00111011_2

2. List the universal gates and draw their symbols.

3. Mention three uses of alphanumeric codes.

4. Draw a BCD to decimal decoder circuit.

5. What is demultiplexer?

6. Draw a level clocked T-flip flop.

7. Define modulus of a counter.

8. Draw a parallel-in parallel-out shift register.

9. Write any three differences between EEPROM and UVPROM.

10. Compare static RAM and dynamic RAM.

PART—B 10×5=50

Instructions : (1) Answer *any* **five** questions.
(2) Each question carries **ten** marks.
(3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. *(a)* Draw the sum of products circuit for the equation $Y \quad (\overline{A} \quad B)(A \quad B)$ and simplify the equation. 5

(b) Write Boolean expressions of sum of minterms from the following truth table and simplify : 5

Input			Output
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

12. (a) Draw the circuit of TTL NAND gate with totem pole output. 5

(b) Compare TTL, CMOS and ECL logic families. 5

13. (a) Draw the logic circuit and truth table of full adder. 5

(b) Draw half-adder circuit using exclusive OR gate and an AND gate and explian its function using truth table. 5

14. Draw a two-bit digital comparator circuit and explain.

15. (a) Draw and explian the operation of NAND latch. 5

(b) Write about level triggering and edge triggering. 5

16. Explain the working of JK flip-flop using truth table.

17. (a) Explain the terms resolution, accuracy and monotonicity of converter. 5

(b) Draw R-2R ladder network D/A converter. 5

18. Describe the successive approximation method of A/D converter with a block diagram.

★ ★ ★