4233

BOARD DIPLOMA EXAMINATION, (C-14)

MARCH /APRIL-2019

DCME - THIRD SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time: 3 Hours] [Max.Marks: 80M

PART-A

3x10=30M

Instructions: 1) Answer **all** questions. Each question carries **three** marks.
2) Answer should be brief and straight to the point and shall not exceed five simple sentences.

1) Write any three postulates of Boolean algebra.

2) Draw logic circuit of half adder with its truth table.

3) Write the differences between parallel adder and serial adder.

4) Write the Classification of different Logic Families?

5) State the need for JK Master Slave Flip Flop.

6) Draw clocked RS Flip Flop with its truth table.

7) Distinguish between Asynchronous and Synchronous counters.

8) Define a Register and state the need of it.

9) Differentate between static RAM and dynamic RAM.

10) List any three applications of Demultiplexers.

PART-B

5x10=50M

Instructions: 1) Answer any **five** questions. Each question carries **ten** marks.
2) The answers should be comprehensive and the criteria for valuation is the content but not the length of answer.

11) a) Explain EX-OR and EX-NOR gates 3

b) Explain Realization of AND, OR, NOT gates using NAND gate only. 5

c) Explain why NAND and NOR are called Universal gates. 2

12) a) Simplify the following expression using K-Map
$Y=\sum m(0,1,2,3,5,7,8,9,10,11,13,14,15)$ 5

b) Explain working of 2's complement Adder Subtractor with neat diagram. 5

13) Draw and explain the working of D Flip-Flop with turth table and timing diagram.

14) Draw and explain the working of JK Master Slave Flip Flop.

15) Draw and explain the operation of a programmable counter.

16) a) Explain briefly the working of DOWN counter with neat diagram. 5

b) Draw and explain the operation of 10 X 4 encoder. 5

17) Explain the data transfer in the following registers with neat diagram.
a) Serial in - Serial out b) Serial in - Paraller out (5+5)

18) Explain the use of shift register as memory with neat diagram. 10

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