C09-CM-304/C09-IT-304

3230

BOARD DIPLOMA EXAMINATION, (C-09)

OCT / NOV-2015

DCM - THIRD SEMESTER EXAMINATION

DIGITAL ELECTRONICS AND COMPUTER ARCHITECTURE

Time : 3 hours] [Total Marks : 80

PART - A 10 X 3 = 30

Instructions : (1) Answer **all** questions.

(2) Each questions carries **three** marks.

(3) Answers should be brief and straight to the point and shall not exceed ***five*** simple sentences.

1. Draw the symbols and truth tables for the followings gates : (a) NAND and (b) NOR

2. Express the Boolean function F=A+B'C in sum of minterms form.

3. What are meant by edge triggering and level triggering in flip-flops?

4. Draw mod-8 ripple counter.

5. What is demultiplexer?

6. Define execution cycle.

7. Give the examples for two-address and three-address instructions.

8. What is meant by instruction format?

9. List any three characteristics of memory devices.

10. What is meant by asynchronous data transfer?

PART - B

10 X 5 = 50

Instructions : (1) Answer *any* **five** questions.

(2) Each question carries **ten** marks.

(3) Answer should be comprehensive and the criteria for valuation is the content but not the length of the answer.

11. Realize the following function using K-map :

$$F(A, B, C, D) = \Sigma m (1, 3, 4, 5, 7, 9, 11, 13, 15)$$

12. Explain the working of RST flip-flop with logic diagram, and write its truth table.

13. Draw and explain 3-bit UP/DOWN synchronous counter.

14. Draw the block diagram of simple accumulator based CPU and explain the function of each unit.

15. Draw and explain the flowchart for division of fixed point numbers.

16. (a) Explain priority interrupt mode of data transfer.

(b) Explain Daisy chain priority interrupt mode of data transfer.

17. (a) Explain the use of a shift register as memory.

(b) Explain the 4 1 multiplexer with diagram.

18. (a) Explain the fixed point representation of numbers with example.

(b) Explain the principle of cache memory.

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