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C09–AEI–305

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BOARD DIPLOMA EXAMINATION, (C–09)

OCT/NOV—2017

DAEI—THIRD SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time : 3 hours] [*Total Marks* : 80

PART—A 3×10=30

Instructions : (1) Answer **all** questions.
(2) Each question carries **three** marks.
(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. Perform the binary addition $(10110)_2$ $(0101\ 1)_2$.

2. Simplify $(A\ \overline{B})(\overline{A}\ B)(\overline{A}\ \overline{B})$.

3. Draw 2's compliment parallel adder/subtractor circuit.

4. Draw half-adder using Ex-OR and AND gates.

5. State the need for preset and clear inputs.

6. Draw *T* flip-flop with truth table.

7. Draw the decade counter using JK flip-flops.

8. Draw the diagram of ring counter.

9. Draw the diagram of RAM cell.

10. Define the term resolution of a D/A converter.

PART—B

10×5=50

Instructions : (1) Answer *any* **five** questions.

(2) Each question carries **ten** marks.

(3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. State any five postulates in Boolean algebra. 10

12. *(a)* Explain the working of NAND and NOR gates using truth tables. 4

(b) Develop AND, OR operations using NAND gates. 6

13. Draw and explain the two-bit digital comparator. 10

14. *(a)* Draw and explain the 4 1 multiplexer circuit with truth table. 7

(b) Draw 2 4 decoder circuit. 3

15. *(a)* Draw and explain RS latch using NAND gates. 5

(b) Differentiate between synchronous and asynchronous SLC. 5

16. Draw and explain 4-bit ripple counter with truth table and timing diagram. 10

17. *(a)* Draw and explain the working of series in parallel-out shift register. 7

(b) Draw the 3-bit shift-right register. 3

18. Explain D/A conversion using R-2R ladder network. 10

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