Instruction Set Features -1

1. In which of these modes, the immediate operand is included in the instruction itself?
a) register operand mode
b) immediate operand mode
c) register and immediate operand mode
d) none of the mentioned
View Answer
Answer: b
Explanation: In immediate operand mode, the immediate operand is included in the instruction itself.

2. In register address mode, the operand is stored in
a) 8-bit general purpose register
b) 16-bit general purpose register
c) si or di
d) all of the mentioned
View Answer
Answer: d
Explanation: In register address mode, the operand is stored either in one of the 8-bit or 16-bit general purpose registers or in SI, DI, BX or BP.

3. In which of the following addressing mode, the offset is obtained by adding displacement and contents of one of the base registers?
a) direct mode
b) register mode
c) based mode
d) indexed mode
View Answer
Answer: c
Explanation: In a based mode, the offset is obtained by adding displacement and contents of one of the base registers, either BX or BP.

4. In which of the following addressing mode, the offset is obtained by adding displacement, with the contents of SI?
a) direct mode
b) register mode
c) based mode
d) indexed mode
View Answer
Answer: d
Explanation: In an indexed mode, the offset is obtained by adding displacement, with contents of an index register, either SI or DI.

5. The address of a location of the operand is calculated by adding the contents of any of the base registers, with the contents of any of index registers in
a) based indexed mode with displacement
b) based indexed mode
c) based mode
d) indexed mode
View Answer
Answer: b
Explanation: In a based indexed mode, the operand is stored at a location, whose

address is calculated by adding the contents of any of the base registers, with the contents of any of the index registers.

6. Which of the following is not a data type of 80286?
a) Ordinal or unsigned
b) ASCII
c) Packed BCD
d) None of the mentioned
View Answer
Answer: d
Explanation: The 80286 supports seven data types. They are
1. integer
2. Ordinal (unsigned)
3. pointer
4. string
5. ASCII
6. BCD
7. Packed BCD.

7. The representation of 8-bit or 16-bit signed binary operands using 2's complement is a data type of
a) Ordinal
b) ASCII
c) Packed BCD
d) integer
View Answer
Answer: d
Explanation: In integer data type, 8-bit or 16-bit signed binary operands are represented using 2's complement.

8. The instruction that pushes the general purpose registers, pointer and index registers on to the stack is
a) POPF
b) PUSH Imd
c) PUSH*A
d) PUSHF
View Answer
Answer: c
Explanation: The PUSH*A instruction, pushes the general purpose registers, AX, CX, DX and BX, pointer and index registers, SP, BP, SI, DI, on to the stack.

9. While executing the PUSH*A instruction, the stack pointer is decremented by
a) 1 bit
b) 2 bits
c) 4 bits
d) 16 bits
View Answer
Answer: b
Explanation: The stack pointer is decremented by 16 (eight 2-byte registers).

10. The statement that is true for the instruction POP*A is
a) flags are unaffected
b) no operands are required
c) exceptions generated are same as that of PUSH*A

d) all of the mentioned
View Answer
Answer: d
Explanation: The POP*A instruction, pops all the contents of the registers DI, SI, BP, SP, BX, DX, CX and AX from the stack in this sequence, that is exactly opposite to that of pushing.

11. The instruction that multiplies the content of AL with a signed immediate operand is
a) MUL
b) SMUL
c) IMUL
d) None of the mentioned
View Answer
Answer: c
Explanation: The IMUL instruction multiplies the content of AL with a signed immediate operand, and the signed 16-bit result is stored in AX.

12. The instruction that represents the ‘rotate source, count’ is
a) RCL
b) RCR
c) ROR
d) All of the mentioned
View Answer
Answer: d
Explanation: The rotate source, count is a group of four instructions containing RCL, RCR, ROL, ROR.

Features of 80586 (Pentium) , Concepts of Computer Architecture , Branch Prediction

1. The salient feature of Pentium is
a) superscalar architecture
b) superpipelined architecture
c) superscalar and superpipelined architecture
d) none of the mentioned
View Answer
Answer: c
Explanation: The salient feature of Pentium is its superscalar, superpipelined architecture.

2. The number of stages of the integer pipeline, U, of Pentium is
a) 2
b) 4
c) 3
d) 6
View Answer
Answer: b
Explanation: The Pentium has two integer pipelines, U and V, where each one is a 4-stage pipeline.

3. Which of the following is a cache of Pentium?
a) data cache
b) data cache and instruction cache
c) instruction cache
d) none of the mentioned
View Answer
Answer: b
Explanation: The Pentium has two separate caches. They are data cache and instruction cache.

4. The speed of integer arithmetic of Pentium is increased to a large extent by
a) on-chip floating point unit
b) superscalar architecture
c) 4-stage pipelines
d) all of the mentioned
View Answer
Answer: c
Explanation: The Pentium has two integer pipelines, U and V, where each one is a 4-stage pipeline. This enhances the speed of integer arithmetic of Pentium to a large extent.

5. For enhancement of processor performance, beyond one instruction per cycle, the computer architects employ the technique of
a) super pipelined technique
b) multiple instruction issue
c) super pipelined technique and multiple instruction issue
d) none of the mentioned
View Answer

Answer: b
Explanation: For enhancement of processor performance, beyond one instruction per cycle, the computer architects employ the technique of multiple instruction issue.

6. Which of the following is a class of architecture of MII (multiple instruction issue)?
a) super pipelined architecture
b) multiple instruction issue
c) very small instruction word architecture
d) super scalar architecture
View Answer
Answer: d
Explanation: The MII architecture may again be classified into two categories:
1. Very long instruction word architecture
2. Superscalar architecture.

7. The compiler reorders the sequential stream of code that is coming from memory into a fixed size instruction group in
a) super pipelined architecture
b) multiple instruction issue
c) very long instruction word architecture
d) super scalar architecture
View Answer
Answer: c
Explanation: In VLIW processors, the compiler reorders the sequential stream of code that is coming from memory into a fixed size instruction group, and issues them in parallel for execution.

8. The architecture in which the hardware decides which instructions are to be issued concurrently at run time is
a) super pipelined architecture
b) multiple instruction issue
c) very long instruction word architecture
d) superscalar architecture
View Answer
9. The CPU has to wait until the execution stage to determine whether the condition is met in
a) unconditional branch
b) conditional branch
c) pipelined execution branch
d) none of the mentioned
View Answer
Answer: b
Explanation: In conditional branch, the CPU has to wait until the execution stage to determine whether the condition is met or not. When the condition satisfies, a branch is to be taken.

10. The memory device that holds branch target addresses for previously executed branches is
a) Tristate buffer
b) RAM
c) ROM

d) Branch target buffer
View Answer
Answer: d
Explanation: The branch target buffer in Pentium CPU holds branch target addresses for previously executed branches.

11. The branch target buffer is
a) four-way set-associative memory
b) has branch instruction address
c) has destination address
d) all of the mentioned
View Answer
Answer: d
Explanation: The branch target buffer is a four-way set-associative memory. Whenever a branch is taken, the CPU enters the branch instruction address, and also the destination address in the branch target buffer.

System Architecture

1. The stage in which the CPU fetches the instructions from the instruction cache in superscalar organization is
a) Prefetch stage
b) D1 (first decode) stage
c) D2 (second decode) stage
d) Final stage
View Answer
Answer: a
Explanation: In the prefetch stage of pipeline, the CPU fetches the instructions from the instruction cache, which stores the instructions to be executed. In this stage, CPU also aligns the codes appropriately.

2. The CPU decodes the instructions and generates control words in
a) Prefetch stage
b) D1 (first decode) stage
c) D2 (second decode) stage
d) Final stage
View Answer
Answer: b
Explanation: In D1 stage, the CPU decodes the instructions and generates control words. For simple RISC instructions, only single control word is enough for starting the execution.

3. The fifth stage of pipeline is also known as
a) read back stage
b) read forward stage
c) write back stage
d) none of the mentioned
View Answer
Answer: c
Explanation: The fifth stage or final stage of pipeline is also known as “Write back (WB) stage”.

4. In the execution stage the function performed is
a) CPU accesses data cache
b) executes arithmetic/logic computations
c) executes floating point operations in execution unit
d) all of the mentioned
View Answer
Answer: d
Explanation: In the execution stage, known as E-stage, the CPU accesses data cache, executes arithmetic/logic computations, and floating point operations in execution unit.

5. The stage in which the CPU generates an address for data memory references in this stage is
a) prefetch stage
b) D1 (first decode) stage
c) D2 (second decode) stage
d) execution stage
View Answer

Answer: c
Explanation: In the D2 (second decode) stage, CPU generates an address for data memory references in this stage. This stage is required where the control word from D1 stage is again decoded for final execution.

6. The feature of separated caches is
a) supports the superscalar organization
b) high bandwidth
c) low hit ratio
d) all of the mentioned
View Answer
Answer: d
Explanation: The separated caches have low hit ratio compared to a unified cache, but have the advantage of supporting the superscalar organization and high bandwidth.

7. In the operand fetch stage, the FPU (Floating Point Unit) fetches the operands from
a) floating point unit
b) instruction cache
c) floating point register file or data cache
d) floating point register file or instruction cache
View Answer
Answer: c
Explanation: In the operand fetch stage, the FPU (Floating Point Unit) fetches the operands from either floating point register file or data cache.

8. The FPU (Floating Point Unit) writes the results to the floating point register file in
a) X1 execution state
b) X2 execution state
c) write back stage
d) none of the mentioned
View Answer
9. The floating point multiplier segment performs floating point multiplication in
a) single precision
b) double precision
c) extended precision
d) all of the mentioned
View Answer
Answer: d
Explanation: The floating point multiplier segment performs floating point multiplication in single precision, double precision and extended precision.

10. The instruction or segment that executes the floating point square root instructions is
a) floating point square root segment
b) floating point division and square root segment
c) floating point divider segment
d) none of the mentioned
View Answer
Answer: c
Explanation: The floating point divider segment executes the floating point division and square root instructions.

11. The floating point rounder segment performs rounding off operation at
a) after write back stage
b) before write back stage

c) before arithmetic operations
d) none of the mentioned
View Answer
Answer: b
Explanation: The results of floating point addition or division process may be required to be rounded off, before write back stage to the floating point registers.

12. Which of the following is a floating point exception that is generated in case of integer arithmetic?
a) divide by zero
b) overflow
c) denormal operand
d) all of the mentioned
View Answer
Answer: d
Explanation: In the case of integer arithmetic, the possible floating point exceptions in Pentium are:
1. divide by zero
2. overflow
3. denormal operand
4. underflow
5. invalid operation.

13. The mechanism that determines whether a floating point operation will be executed without creating any exception is
a) Multiple Instruction Issue
b) Multiple Exception Issue
c) Safe Instruction Recognition
d) Safe Exception Recognition
View Answer
Answer: c
Explanation: A mechanism known as Safe Exception Recognition (SER) had been employed in Pentium which determines whether a floating point operation will be executed without creating any exception.

Enhanced Instruction Set of Pentium, Intel

MMX Architecture

1. Which of the following is not a transcendental instruction?
a) FSIN
b) FCOS
c) FMUL
d) FPTAN
View Answer
Answer: c
Explanation: The FMUL instruction is a float point multiplication, which is not a transcendental instruction.

2. The transcendental instruction that supports computation of sine and cosine is
a) FCOSSIN
b) FSNE
c) FSINFCOS
d) FSINCOS
View Answer
Answer: d
Explanation: The instruction, FSINCOS, supports to compute sine and cosine.

3. The instruction that computes tan(x) is
a) FTAN
b) FTNGNT
c) FPTAN
d) FXTAN
View Answer
Answer: c
Explanation: The instruction, FPTAN, computes tan(x).

4. The instruction that computes arctan(x) is
a) FTAN
b) FACTN
c) FARCTAN
d) FPATAN
View Answer
Answer: d
Explanation: The instruction, FPATAN, computes arctan(x) which is arc tangent of x.

5. The instruction, F2XMI, is used to compute
a) 2X
b) 2X-1
c) 2X+1
d) 2X+2
View Answer
Answer: b
Explanation: The instruction, F2XMI, is used to compute 2X-1.

6. The instruction, FYL2XP, supports to compute the expression
a) Y*logX
b) Y*log2X
c) Y*log(2X+1)
d) Y*log2(X+1)
View Answer
Answer: d
Explanation: The instruction, FYL2XP, supports to compute the expression Y*log2(X+1).

7. The size of a general purpose floating point register of floating point unit is
a) 4 bytes
b) 40 bytes
c) 8 bytes
d) 80 bits
View Answer
Answer: d
Explanation: There are eight general purpose floating point registers in the floating point unit. Each of these eight registers are of 80-bits width.

8. For floating point operations, the bits used by mantissa in a floating point register is
a) 32
b) 64
c) 72
d) 79
View Answer
Answer: b
Explanation: For floating point operations, 64 bits are used for the mantissa, and the rest 16 bits for exponent.

9. The multimedia applications mainly require the architecture of
a) single instruction stream single data stream
b) multiple instruction stream single data stream
c) single instruction stream multiple data stream
d) multiple instruction stream multiple data stream
View Answer
Answer: c
Explanation: Most of the multimedia applications mainly require the architecture of single instruction stream multiple data stream.

10. The size of each MMX (Multimedia Extension) register is
a) 32 bits
b) 64 bits
c) 128 bits
d) 256 bits
View Answer
Answer: b
Explanation: The MMX registers use only the 64-bit mantissa portion of the general purpose floating point registers, to store MMX operands. Thus, the MMX programmers virtually get eight new MMX registers, each of 64 bits.

11. After a sequence of MMX instructions is executed, the MMX registers should be cleared by an instruction,
a) CLEAR
b) RESET

c) EMM
d) EMMS
View Answer
Answer: d
Explanation: After a sequence of MMX instructions is executed, the MMX registers should be cleared by an instruction, EMMS, which implies Empty the MMX Stack.

12. The number of pixels that can be manipulated in a single register by the CPU using MMX architecture is
a) 4
b) 6
c) 8
d) 10
View Answer
Answer: c
Explanation: Any CPU can manipulate only one pixel at a time. But by using MMX architecture, we can manipulate eight such pixels, packed in a single 64-bit register.

13. After executing the floating point instructions, the floating point registers should be cleared by an instruction,
a) CLEAR
b) EFPR
c) EMMF
d) EMMS
View Answer
Answer: d
Explanation: After executing the floating point instructions, the floating point registers should be cleared by an instruction, EMMS.