Interrupts and Interrupt Service Routines

1. While CPU is executing a program, an interrupt exists then it
a) follows the next instruction in the program
b) jumps to instruction in other registers
c) breaks the normal sequence of execution of instructions
d) stops executing the program
View Answer
Answer: c
Explanation: An interrupt function is to break the sequence of operation.

2. An interrupt breaks the execution of instructions and diverts its execution to
a) Interrupt service routine
b) Counter word register
c) Execution unit
d) control unit
View Answer
Answer: a
Explanation: An interrupt transfers the control to interrupt service routine (ISR). After executing ISR, the control is transferred back again to the main program.

3. While executing the main program, if two or more interrupts occur, then the sequence of appearance of interrupts is called
a) multi-interrupt
b) nested interrupt
c) interrupt within interrupt
d) nested interrupt and interrupt within interrupt
View Answer
Answer: d
Explanation: If an interrupt occurs while executing a program, and the processor is executing the interrupt, if one more interrupt occurs again, then it is called a nested interrupt.

4. Whenever a number of devices interrupt a CPU at a time, and if the processor is able to handle them properly, it is said to have
a) interrupt handling ability
b) interrupt processing ability
c) multiple interrupt processing ability
d) multiple interrupt executing ability
View Answer
Answer: c
Explanation: The processor if handles more devices as interrupts then it has multiple interrupt processing ablility

5. NMI stands for
a) nonmaskable interrupt
b) nonmultiple interrupt
c) nonmovable interrupt
d) none of the mentioned
View Answer
Answer: a
Explanation: NMI is the acronym for nonmaskable interrupt.

6. If any interrupt request given to an input pin cannot be disabled by any means then the input pin is called
a) maskable interrupt
b) nonmaskable interrupt
c) maskable interrupt and nonmaskable interrupt
d) none of the mentioned
View Answer
Answer: b
Explanation: A nonmaskable interrupt input pin is one which means that any interrupt request at NMI (nonmaskable interrupt) input cannot be masked or disabled by any means.

7. The INTR interrupt may be
a) maskable
b) nonmaskable
c) maskable and nonmaskable
d) none of the mentioned
View Answer
Answer: a
Explanation: the INTR (interrupt request) is maskable or can be disabled.

8. The Programmable interrupt controller is required to
a) handle one interrupt request
b) handle one or more interrupt requests at a time
c) handle one or more interrupt requests with a delay
d) handle no interrupt request
View Answer
Answer: b
Explanation: If more than one interrupt request (INTR) occurs at a time, then an external chip called programmable interrupt controller is required to handle them.

9. The INTR interrupt may be masked using the flag
a) direction flag
b) overflow flag
c) interrupt flag
d) sign flag
View Answer
Answer: c
Explanation: If a microprocessor wants to serve any interrupt then interrupt flag, IF=1. If interrupt flag, IF=0, then the processor ignores the service.

Interrupt Cycle of 8086/8088

1. If an interrupt is generated from outside the processor then it is an
a) internal interrupt
b) external interrupt
c) interrupt
d) none of the mentioned
View Answer
Answer: b
Explanation: If an external device or a signal interrupts the processor from outside then it is an external interrupt.

2. If the interrupt is generated by the execution of an interrupt instruction then it is
a) internal interrupt
b) external interrupt
c) interrupt-in-interrupt
d) none of the mentioned
View Answer
Answer: a
Explanation: The internal interrupt is generated internally by the processor circuit or by the execution of an interrupt instruction.

3. Example of an external interrupt is
a) divide by zero interrupt
b) keyboard interrupt
c) overflow interrupt
d) type2 interrupt
View Answer
Answer: b
Explanation: Since the keyboard is external to the processor, it is an external interrupt.

4. Example of an internal interrupt is
a) divide by zero interrupt
b) overflow interrupt
c) interrupt due to INT
d) all of the mentioned
View Answer
Answer: d
Explanation: Since the interrupts occur within the processor itself, they are called internal interrupts.

5. The interrupt request that is independent of IF flag is
a) NMI
b) TRAP
c) Divide by zero
d) All of the mentioned
View Answer
Answer: d
Explanation: These requests are independent of IF flag

6. The type of the interrupt may be passed to the interrupt structure of CPU from
a) interrupt service routine
b) stack

c) interrupt controller
d) none of the mentioned
View Answer
Answer: c
Explanation: After an interrupt is acknowledged, the CPU computes the vector address from the type of the interrupt that may be passed to the internal structure of the CPU from an interrupt controller in case of external interrupts.

7. During the execution of an interrupt, the data pushed into the stack is the content of
a) IP
b) CS
c) PSW
d) All of the mentioned
View Answer
8. After every response to the single step interrupt the flag that is cleared is
a) IF (Interrupt Flag)
b) TF (Trap Flag)
c) OF (Overflow Flag)
d) None of the mentioned
View Answer
Answer: b
Explanation: If the trap flag is set then the processor enters the single step execution mode. After the execution, the trap flag is cleared.

9. At the end of ISR, the instruction should be
a) END
b) ENDS
c) IRET
d) INTR
View Answer
Answer: c
Explanation: After the execution of the ISR, the control must go to the previous program (maybe main program) which was being executed. To execute it, IRET is placed at the end of ISR.

10. When the CPU executes IRET,
a) contents of IP and CS are retrieved
b) the control transfers from ISR to main program
c) clears the trap flag
d) clears the interrupt flag
View Answer
Answer: a
Explanation: When the instruction IRET is executed, the contents of flags, IP and CS which were saved at the stack by the CALL instruction are retrieved to the respective registers.

Non Maskable Interrupt and Maskable Interrupt (INTR)

1. The interrupt for which the processor has the highest priority among all the external interrupts is
a) keyboard interrupt
b) TRAP
c) NMI
d) INT
View Answer
Answer: c
Explanation: The Non-Maskable Interrupt input pin has the highest priority among all the external interrupts.

2. The interrupt for which the processor has highest priority among all the internal interrupts is
a) keyboard interrupt
b) TRAP
c) NMI
d) INT
View Answer
Answer: b
Explanation: TRAP is the internal interrupt that has highest priority among all the interrupts except the Divide By Zero (Type 0) exception.

3. In case of string instructions, the NMI interrupt will be served only after
a) initialisation of string
b) execution of some part of the string
c) complete string is manipulated
d) the occurrence of the interrupt
View Answer
Answer: c
Explanation: When NMI is activated, the current instruction being executed is completed and then NMI is served. In the case of string instructions, it is served after the complete string is manipulated.

4. The NMI pin should remain high for atleast
a) 4 clock cycles
b) 3 clock cycles
c) 1 clock cycle
d) 2 clock cycles
View Answer
Answer: d
Explanation: The NMI pin should remain high for atleast 2 clock cycles and need not be synchronized with the clock for being sensed.

5. The INTR signal can be masked by resetting the
a) TRAP flag
b) INTERRUPT flag
c) MASK flag
d) DIRECTION flag
View Answer
Answer: b
Explanation: The INTR signal can be masked by resetting the interrupt flag.

6. For the INTR signal, to be responded to in the next instruction cycle, it must go _____ in the last clock cycle of the current instruction
a) high
b) low
c) high or low
d) unchanged
View Answer
Answer: a
Explanation: The INTR signal must go high in the clock cycle of the current instruction in order to respond in the next instruction cycle.

7. The status of the pending interrupts is checked at
a) the end of main program
b) the end of all the interrupts executed
c) the beginning of every interrupt
d) the end of each instruction cycle
View Answer
Answer: d
Explanation: At the end of each instruction, the status of the pending interrupts is checked.

8. Once the processor responds to an INTR signal, the IF is automatically
a) set
b) reset
c) high
d) low
View Answer
Answer: b
Explanation: The IF is automatically reset when the processor responds to an INTR signal. If the processor wants to respond to any type of INTR signal further then, the IF should again be set.

9. If the pin LOCK (active low based) is low at the trailing edge of the first ALE pulse, then till the start of the next machine cycle, the pin LOCK (active low) is
a) low
b) high
c) low or high
d) none of the mentioned
View Answer
Answer: a
Explanation: The pin LOCK (active low) remains low till the start of the next machine cycle.

10. With the trailing edge of the LOCK (active low), the INTA (active low) goes low and remains in it for
a) 0 clock cycle
b) 1 clock cycle
c) 2 clock cycles
d) 3 clock cycles
View Answer
Answer: c
Explanation: The INTA (active low) goes low and remains low for two clock cycles before returning back to the high state.

Interrupt Programming, Passing Parameters to Procedures, Handling Programs of Size More Than 64KB

1. The method of defining the interrupt service routine for software is
a) same as that of hardware
b) difficult than hardware
c) easier than software
d) none of the mentioned
View Answer
Answer: a
Explanation: For both software and hardware, the method of defining the interrupt service routine is the same.

2. While programming for any type of interrupt, the interrupt vector table is set
a) externally
b) through a program
c) either externally or through the program
d) externally and through the program
View Answer
Answer: c
Explanation: The programmer must, either externally or through the program, set the interrupt vector table for that type preferably with the CS and IP addresses of the interrupt service routine.

3. To execute a program one should
a) assemble the program
b) link the program
c) apply external pulse
d) all of the mentioned
View Answer
Answer: d
Explanation: To execute a program, first assemble it, link it and then execute it. After execution, a new file RESULT is created in the directory. Then external pulse is applied to IRQ2 pin, and this will again cause the execution of ISR into the file.

4. Procedures are also known as
a) macros
b) segment
c) subroutines
d) none
View Answer
Answer: c
Explanation: Procedures are also known as subroutines.

5. Procedures, for their execution, require
a) input data
b) output data
c) constants

d) input data or constants
View Answer
Answer: d
Explanation: Procedures require input data or constants for their execution. Their data or constants may be passed to the subroutine by the main program.

6. The technique that is used to pass the data or parameter to procedures in assembly language program is by using
a) global declared variable
b) registers
c) stack
d) all of the mentioned
View Answer
Answer: d
Explanation: The techniques that are used to pass the data or parameter to procedures are by using global declared variable, registers of CPU, memory locations, stack, PUBLIC & EXTRN.

7. If a procedure is interactive, then
a) it accepts inputs directly from input devices
b) it uses global declared variable technique
c) it uses stack
d) it uses memory locations
View Answer
Answer: a
Explanation: If a procedure is interactive, then it accepts the inputs directly from input devices.

8. For passing the parameters to procedures using the PUBLIC & EXTRN directives, it must be declared PUBLIC in the
a) subroutine
b) procedure
c) main routine
d) main routine and subroutine
View Answer
Answer: c
Explanation: For passing the parameters to procedures, it must be declared PUBLIC in the main routine and the same should be declared EXTRN in the procedure.

9. The technique to estimate the size of an executable program, before it is assembled and linked is
a) memory location technique
b) global variable technique
c) stack
d) none
View Answer
Answer: d
Explanation: There is no technique to estimate the size of an executable program before it is assembled and linked.

10. To estimate the size of an executable program before it is assembled and linked, the programming methodology concerned is by writing
a) programs with more than one segment for data and code
b) programs with FAR subroutines each of size up to 64KB

c) programs with more than one segment for stack
d) all of the mentioned
View Answer
Answer: d
Explanation: By writing programs with more than one segment for data, code or stack or by writing programs with FAR subroutines each of size 64KB, the size of an executable program can be estimated.