

Addressing Modes of 8086

1. The instruction, MOV AX, 0005H belongs to the address mode

- a) register
- b) direct
- c) immediate
- d) register relative

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Answer: c

Explanation: In Immediate addressing mode, immediate data is a part of instruction and appears in the form of successive byte or bytes.

2. The instruction, MOV AX, 1234H is an example of

- a) register addressing mode
- b) direct addressing mode
- c) immediate addressing mode
- d) based indexed addressing mode

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Answer: c

Explanation: Since immediate data is present in the instruction.

3. The instruction, MOV AX, [2500H] is an example of

- a) immediate addressing mode
- b) direct addressing mode
- c) indirect addressing mode
- d) register addressing mode

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Answer: b

Explanation: Since the address is directly specified in the instruction as a part of it.

4. If the data is present in a register and it is referred using the particular register, then it is

- a) direct addressing mode
- b) register addressing mode
- c) indexed addressing mode
- d) immediate addressing mode

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Answer: b

Explanation: Since register is used to refer the address.

5. The instruction, MOV AX,[BX] is an example of

- a) direct addressing mode
- b) register addressing mode
- c) register relative addressing mode
- d) register indirect addressing mode

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Answer: d

Explanation: Since the register used to refer to the address is accessed indirectly.

6. If the offset of the operand is stored in one of the index registers, then it is

- a) based indexed addressing mode
- b) relative based indexed addressing mode
- c) indexed addressing mode

d) none of the mentioned

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Answer: c

Explanation: In the indexed addressing mode, the offset of an operand is stored and in the rest of them, address is stored.

7. The addressing mode that is used in unconditional branch instructions is

- a) intrasegment direct addressing mode
- b) intrasegment indirect addressing mode
- c) intrasegment direct and indirect addressing mode
- d) intersegment direct addressing mode

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Answer: b

Explanation: In intrasegment indirect mode, the branch address is found as the content of a register or a memory location.

8. If the location to which the control is to be transferred lies in a different segment other than the current one, then the mode is called

- a) intrasegment mode
- b) intersegment direct mode
- c) intersegment indirect mode
- d) intersegment direct and indirect mode

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Answer: d

Explanation: In intersegment mode, the control to be transferred lies in a different segment.

9. The instruction, JMP 5000H:2000H; is an example of

- a) intrasegment direct mode
- b) intrasegment indirect mode
- c) intersegment direct mode
- d) intersegment indirect mode

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Answer: c

Explanation: Since in intersegment direct mode, the address to which the control is to be transferred is in a different segment.

10. The contents of a base register are added to the contents of index register in

- a) indexed addressing mode
- b) based indexed addressing mode
- c) relative based indexed addressing mode
- d) based indexed and relative based indexed addressing mode

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Answer: d

Explanation: The effective address is formed by adding the contents of both base and index registers to a default segment

Instruction Set of 8086/8088 -1

1. The instruction that is used to transfer the data from source operand to destination operand is

- a) data copy/transfer instruction
- b) branch instruction
- c) arithmetic/logical instruction
- d) string instruction

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Answer: a

Explanation: These instructions are used to copy and transfer the instructions.

2. Which of the following is not a data copy/transfer instruction?

- a) MOV
- b) PUSH
- c) DAS
- d) POP

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Answer: c

Explanation: DAS (Decimal Adjust after Subtraction) is an arithmetic instruction.

3. The instructions that involve various string manipulation operations are

- a) branch instructions
- b) flag manipulation instructions
- c) shift and rotate instructions
- d) string instructions

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Answer: d

Explanation: The string instructions perform operations on strings such as load, move, scan, compare etc.

4. Which of the following instruction is not valid?

- a) MOV AX, BX
- b) MOV DS, 5000H
- c) MOV AX, 5000H
- d) PUSH AX

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Answer: b

Explanation: Both the source and destination operands cannot be memory locations except for string instructions.

5. In PUSH instruction, after each execution of the instruction, the stack pointer is

- a) incremented by 1
- b) decremented by 1
- c) incremented by 2
- d) decremented by 2

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Answer: d

Explanation: The actual current stack-top is always occupied by the previously pushed data. So, the push operation decrements SP by 2 and then stores the two bytes contents of the operand onto the set

6. The instruction that pushes the contents of the specified register/memory location on to the stack is

- a) PUSHF
- b) POPF
- c) PUSH
- d) POP

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Answer: c

Explanation: Since PUSH operation transfers data to stack from a register or memory location.

7. In POP instruction, after each execution of the instruction, the stack pointer is

- a) incremented by 1
- b) decremented by 1
- c) incremented by 2
- d) decremented by 2

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Answer: c

Explanation: The actual current stack top is popped into the specific operand as the contents of stack top memory is stored in AL&SP and further contents of the memory location pointed to by SP are copied to AH & SP.

8. The instructions that are used for reading an input port and writing an output port respectively are

- a) MOV, XCHG
- b) MOV, IN
- c) IN, MOV
- d) IN, OUT

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Answer: d

Explanation: The address of the input/output port may be specified directly or indirectly. Example for input port: IN AX, DX; This instruction reads data from a 16-bit port whose address is in DX and stores it in AX

Example for output port: OUT 03H, AL; This sends data available in AL to a port whose address is 03H.

9. The instruction that is used for finding out the codes in case of code conversion problems is

- a) XCHG
- b) XLAT
- c) XOR
- d) JCXZ

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10. The instruction that loads effective address formed by destination operand into the specified source register is

- a) LEA
- b) LDS
- c) LES
- d) LAHF

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Answer: a

Explanation: The instruction, LEA loads effective address and is more useful for assembly language rather than for machine language.

11. The instruction that loads the AH register with the lower byte of the flag register is

- a) SAHF
- b) AH
- c) LAHF
- d) PUSHF

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Answer: c

Explanation: The instruction LAHF(Load AH from a lower byte of Flag) may be used to observe the status of all the condition code flags(except overflow flag) at a time.

12. The instruction that pushes the flag register on to the stack is

- a) PUSH
- b) POP
- c) PUSHF
- d) POPF

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Answer: c

Explanation: The instruction PUSHF(push flags to stack) pushes the flag register on to the stack.

13. The instruction that loads the flag register completely from the word contents of the memory location is

- a) PUSH
- b) POP
- c) PUSHF
- d) POPF

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Answer: d

Explanation: POPF is pop flags to stack.

14. The instruction that adds immediate data/contents of the memory location specified in an instruction/register to the contents of another register/memory location is

- a) SUB
- b) ADD
- c) MUL
- d) DIV

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Answer: b

Explanation: ADD instruction adds the data.

15. The instruction that supports addition when carry exists is

- a) ADD
- b) ADC
- c) ADD & ADC
- d) None of the mentioned

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Answer: b

Explanation: ADC(Add with Carry) instruction performs the same operation as ADD operation, but adds the carry flag bit to the result.

Instruction Set of 8086/8088 – 2

1. The instruction, "INC" increases the contents of the specified register or memory location by

- a) 2
- b) 0
- c) 1
- d) 3

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Answer: c

Explanation: This instruction adds 1 to the contents of the operand and so increments by 1.

2. The instruction that subtracts 1 from the contents of the specified register/memory location is

- a) INC
- b) SUBB
- c) SUB
- d) DEC

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Answer: d

Explanation: The DEC instruction decrements the contents of a specified register/memory location by 1.

3. The instruction that enables subtraction with borrow is

- a) DEC
- b) SUB
- c) SBB
- d) None of the mentioned

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Answer: c

Explanation: The SBB instruction subtracts the source operand and the borrow flag from the destination operand.

4. The flag that acts as Borrow flag in the instruction, SBB is

- a) direction flag
- b) carry flag
- c) parity flag
- d) trap flag

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Answer: b

Explanation: If borrow exists in the subtraction operation performed then carry flag is set.

5. In general, the source operand of an instruction can be

- a) memory location
- b) register
- c) immediate data
- d) all of the mentioned

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Answer: d

Explanation: The source operand is the element which is data or data stored memory location on which operation is performed.

6. In general, the destination operand of an instruction can be

- a) memory location
- b) register
- c) immediate data
- d) memory location and register

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Answer: d

Explanation: Since the destination should be able to store the data, immediate data cannot be considered as a destination operand.

7. The instruction, CMP to compare source and destination operands it performs

- a) addition
- b) subtraction
- c) division
- d) multiplication

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Answer: b

Explanation: For comparison, the instruction CMP subtracts source operand from destination operand.

8. During comparison operation, the result of comparing or subtraction is stored in

- a) memory
- b) registers
- c) stack
- d) no where

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Answer: d

Explanation: The result of subtraction operation is not stored anywhere during a comparison.

9. The instruction that converts the result in an unpacked decimal digits is

- a) AAA
- b) AAS
- c) AAM
- d) All of the mentioned

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Answer: d

Explanation: All the ASCII adjust instructions give result in unpacked decimal form and so are called as "Unpacked BCD arithmetic instructions".

10. Which of the following is a mnemonic?

- a) ADD
- b) ADC
- c) AAA
- d) ADD & ADC

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Answer: c

Explanation: AAA is a mnemonic. It doesn't have either a source or destination operand.

11. The instruction in which adjustment is made before performing the operation is

- a) AAA
- b) AAS
- c) AAM
- d) AAD

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Answer: d

Explanation: The AAD instruction converts two unpacked BCD digits in AH and AL to the equivalent binary number in AL. This adjustment must be made before dividing the two unpacked BCD digits.

12. The expansion of DAA is

- a) decimal adjust after addition
- b) decimal adjust before addition
- c) decimal adjust accumulator
- d) decimal adjust auxiliary

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Answer: c

Explanation: This instruction performs conversion operation.

13. The instruction that is used to convert the result of the addition of two packed BCD numbers to a valid BCD number is

- a) DAA
- b) DAS
- c) AAA
- d) AAS

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Answer: a

Explanation: In this conversion, the result has to be only in AL.

14. The ROR instruction rotates the contents of the destination operand to

- a) left
- b) right
- c) left and then right
- d) right and then left

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Answer: b

Explanation: ROR stands for Rotate Right without carry. so, the instruction rotates right.

Instruction Set of 8086/8088 – 3

1. The mnemonic that is placed before the arithmetic operation is performed is

- a) AAA
- b) AAS
- c) AAM
- d) AAD

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Answer: d

Explanation: The AAD instruction converts two unpacked BCD digits in AH and AL to the equivalent binary number in AL.

2. The Carry flag is undefined after performing the operation

- a) AAA
- b) ADC
- c) AAM
- d) AAD

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Answer: d

Explanation: Since the operation, AAD is performed before division operation is performed, the carry flag, auxiliary flag and overflow flag are undefined.

3. The instruction that performs logical AND operation and the result of the operation is not available is

- a) AAA
- b) AND
- c) TEST
- d) XOR

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Answer: c

Explanation: In the TEST instruction, the logical AND operation is performed and the result is not stored but flags are affected.

4. In the RCL instruction, the contents of the destination operand undergo function as

- a) carry flag is pushed into LSB & MSB is pushed into the carry flag
- b) carry flag is pushed into MSB & LSB is pushed into the carry flag
- c) auxiliary flag is pushed into LSB & MSB is pushed into the carry flag
- d) parity flag is pushed into MSB & LSB is pushed into the carry flag

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Answer: a

Explanation: In RCL(Rotate right through carry), for each operation, the carry flag is pushed into LSB and the MSB of the operand is pushed into carry flag.

5. The instruction that is used as prefix to an instruction to execute it repeatedly until the CX register becomes zero is

- a) SCAS
- b) REP
- c) CMPS
- d) STOS

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Answer: b

Explanation: The instruction to which the REP is prefix, is executed repeatedly until CX

register becomes zero. When CX becomes zero, the execution proceeds to the next instruction in sequence.

6. Match the following

A) MOVSB/SW	1) loads AL/AX register by content of a string
B) CMPS	2) moves a string of bytes stored in source to destination
C) SCAS	3) compares two strings of bytes or words whose length is stored in CX register
D) LODS	4) scans a string of bytes or words

- a) A-3,B-4,C-2,D-1
- b) A-2,B-1,C-4,D-3
- c) A-2,B-3,C-1,D-4
- d) A-2,B-3,C-4,D-1

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Answer: d

Explanation: By using the string instructions, the operations on strings can be performed.

7. The instructions that are used to call a subroutine from the main program and return to the main program after execution of called function are

- a) CALL, JMP
- b) JMP, IRET
- c) CALL, RET
- d) JMP, RET

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Answer: c

Explanation: At each CALL instruction, the IP and CS of the next instruction are pushed onto the stack, before the control is transferred to the procedure. At the end of the procedure, the RET instruction must be executed to retrieve the stored contents of IP & CS registers from a stack.

8. The instruction that unconditionally transfers the control of execution to the specified address is

- a) CALL
- b) JMP
- c) RET
- d) IRET

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Answer: b

Explanation: In this the control transfers to the address specified in the instruction and flags are not affected by this instruction.

9. Which instruction cannot force the 8086 processor out of 'halt' state?

- a) Interrupt request
- b) Reset
- c) Both interrupt request and reset
- d) Hold

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Answer: d

Explanation: Only an interrupt request or Reset will force the 8086 processor to come out of the 'halt' state.

10. NOP instruction introduces

- a) Address
- b) Delay
- c) Memory location
- d) None of the mentioned

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Answer: b

Explanation: NOP is the No operation. It means that the processor performs no operation for the clock cycle and thus there exists a delay.

11. Which of the following is not a machine controlled instruction?

- a) HLT
- b) CLC
- c) LOCK
- d) ESC

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Answer: b

Explanation: Since CLC is a flag manipulation instruction where CLC stands for Clear Carry Flag.

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