COMPUTER ARCHITECTURE BASICS

1.The _____ format is usually used to store data .

a.BCD b. Decimal c. Hexadecimal d. Octal

2. The 8-bit encoding format used to store data in a computer is _____ .

a. ASCII b. EBCDIC c. ANCI d. USCII

3. A source program is usually in _____ .

a. Assembly language b. Machine level language.

c. High-level language. d. Natural language

4.Which memory device is generally made of semi-conductors ?

a. RAM b .Hard-disk c. Floppy disk d. Cd disk

5.The small extremely fast, RAM's are called as _____ .

a. Cache b. Heaps c. Accumulators d. Stacks

6. The ALU makes use of _____ to store the intermediate results .

a. Accumulators b. Registers c. Heap d. Stack

7. The control unit controls other units by generating ____ .

a. Control signals b. Timing signals c. Transfer signals d. Command Signals

8._____ are numbers and encoded characters, generally used as operands .

a. Input b .Data c. Information d. Stored Values

9.The Input devices can send information to the processor,

a. When the SIN status flag is set b. When the data arrives regardless of the SIN flag

c. Neither of the cases d. Either of the cases

10. _____ bus structure is usually used to connect I/O devices .

a. Single b. Multiple c. Star d. Ra

11.The I/O interface required to connect the I/O device to the bus consists of _____

a. Address decoder and registers b. Control circuits

c. Both a and b d. Only b

12. To reduce the memory access time we generally make use of _____ .

a. Heaps b. Higher capacity RAM's c. SDRAM's d. Cache's

13._____ is generally used to increase the apparent size of physical memory .

a. Secondary memory b. Virtual memory c. Hard-disk d. Disks

14.MFC stands for

a. Memory Format Caches. b. Memory Function Complete.

c. Memory Find Command. d. Mass Format Command.

15. The time delay between two successive initiation of memory operation _____ .

a. Memory access time b. Memory search time

c. Memory cycle time d. Instruction delay

16.The decoded instruction is stored in _____ .

a.IR b. PC c. Registers d.MDR

17.The instruction -> Add LOCA,R0 does,

a. Adds the value of LOCA to R0 and stores in the temp register

b. Adds the value of R0 to the address of LOCA

c. Adds the values of both LOCA and R0 and stores it in R0

d. Adds the value of LOCA with a value in accumulator and stores it in R0

18. Which registers can interact with the secondary storage ?

a.MAR b. PC c.IR d.R0

19.During the execution of a program which gets initialized first ?

a.MDR b.IR c. PC d.MAR

20. Which of the register/s of the processor is/are connected to Memory Bus ?

a. PC b.MAR c.IR d. Both a and b

21. ISP stands for,

A .Instruction Set Processor b. Information Standard Processing

c. Interchange Standard Protocol d. Interrupt Service Procedure

22. The internal Components of the processor are connected by _____ .

a. Processor intra-connectivity circuitry b. Processor bus

c. Memory bus d. Rambus

23._____ is used to choose between increment the PC or performing ALU operations .

a. Conditional codes b. Multiplexer c. Control unit d. None of these

24. The registers, ALU and the interconnection between them are collectively called as_____ .

a. Process route b. Information trail c. Information path d. Data path

25._____ is used to store data in registers .

a. D flip flop b. JK flip flop c. RS flip flop d. none of these

26. During the execution of the instructions, a copy of the instructions is placed in the _____

a. Register b.RAM c. System heap d. Cache

27. Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster ?

a. A b. B c. Both take the same time d. Insuffient information

28.A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____ .

a. S uper-scaling b. Pipe-lining c. Parallel Computation d. None of these

29. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution ?

a. ISA b. ANSA c. Super-scalar d. All of the above

30. The clock rate of the processor can be improved by

a. Improving the IC technology of the logic circuits

b. Reducing the amount of processing done in one step

c. By using overclocking method

d. All of the above

31. An optimizing Compiler does,

a. Better compilation of the given piece of code.

b. Takes advantage of the type of processor and reduces its process time.

c. Does better memory management.

d. Both a and c

32. SPEC stands for,

a. Standard Performance Evaluation Code. b. System Processing Enhancing Code.

c. System Performance Evaluation Corporation. d. Standard Processing Enhancement Corporation.

33.As of 2000, the reference system to find the performance of a system is_____ .

a. Ultra SPARC 10 b. SUN SPARC c. SUN II d. None of these

34.When Performing a looping operation, the instruction gets stored in the _____ .

a. Registers b. Cache c. System Heap d. System stack

35.The average number of steps taken to execute the set of instructions can be made to be less than one by following _____ .

a.ISA b. Pipe-lining c. Super-scaling d. Sequential

36.If the instruction, Add R1,R2,R3 is executed in a system which is pipe-lined, then the value of S is (Where S is term of the Basic performance equation)

a.3 b.~2 c.~1 d.6

37.CISC stands for

a. Complete Instruction Sequential Compilation b. Computer Integrated Sequential Compiler

c. Complex Instruction Set Computer d. Complex Instruction Sequential Compilation

38.As of 2000, the reference system to find the SPEC rating are built with _____ Processor .

a. Intel Atom SParc 300Mhz b. Ultra SPARC -IIi 300MHZ

c. Amd Neutrino series d. ASUS A series 450 Mhz

39.I n Breakpoint mode of operation,

a. The program is interrupted after each detection

b. The program will not be stopped and the errors are sorted out after the complete program is scanned

c. There is no effect on the program, i.e the program is executed without rectification of errors

d. The program is alted only at specific points

40.The different modes of operation of a computer is

a. User and System mode b. User and Supervisor mode

c. Supervisor and Trace mode d. Supervisor, User and Trace mode

41.The instructions which can be run only supervisor mode are

a. Non-privileged instructions b. System instructions

c. Privileged instructions d. Exception instructions

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42. A privilege exception is raised,

a. When a process tries to change the mode of the system

b. When a process tries to change the piority level of the other processes

c. When a process tries to access the memory allocated to other user

d. All of the above

43. How is a privilege exception dealt ?

a. The program is alted and the system switches into supervisor mode and restarts the program execution

b. The Program is stopped and removed from the queue

c. The system switches the mode and starts the execution of a new process

d. The system switches mode and runs the debugger

44. After reset, CPU begins execution of instruction from memory address

a.0101H b.8000H c.0000H d. FFFFH

45. Synchronous means _____

a. At irregular intervals b. At same time c. At variable time d. None of these

46.An effective solution to the power consumption problem lies in using _____ transistors to implement ICs.

a. NMOS b.TTL shottky c. PMOS d. both NMOS & PMOS

47. When CPU is executing a Program that is part of the Operating System, it is said to be in

a. Interrupt mode b. System mode c. Half mode d. Simplex mode

48.When a logic circuit diagram is given, you can analyse the circuit to obtain the _____.

a. Result b. Input c. Logic Expression d. None of the above

49.IC chips based on packaging density are

a. Small-Scale Integration (SSI): Up to 12 gates

b. Medium-Scale Integration (MSI): 12–99 gates

c. Small- Scale Integration (SSI): Up to 14 gates

d. Both a and b

50. While designing a digital system, the main objectives are

a. Low cost b. Less number of gates c. Increased Speed d. All of the above

ANSWERS:

1.A 2.B 3.C 4.A 5.A 6.A 7.B 8.B 9.A 10.A 11.C 12.D 13.B 14.B 15.C 16.A 17.C 18.A 19.C 20.B 21.A 22.B 23.B 24.D 25.A 26.D 27.A 28.B 29.C 30.D 31.B 32.C 33.A 34.B 35.C 36.C 37.C 38.B 39.D 40.B 41.C 42.D 43.A 44.C 45.B 46.D 47.B 48.C 49.D 50.D

51.There are two types of parity

a. True and False b.0 and 1 c. Even and Odd d. None of the above

52.This is the maximum time from the start of the valid address of the read cycle to the time when the valid data is available at the data output.

a. Read cycle time (tRC) b. Access time (tA)

c. Read to output valid time (tRD) d. None of the above

53.In a sequential memory, the words are stored in and out in a sequence.

a. Write b. Read c. Write/Read d. All of the above

54.A_____ is a semiconductor memory device used to store information, which is permanent in nature.

a. Last table b.RAM c. K- Map d.ROM

55. Erasing EPROM programming is accomplished by using ultraviolet light that belongs to the UVC range and has a frequency of _____.

a.254.9 b.253.2 c.253.7 d. None of the above

56.The EPROM eraser will emit_____ light.

a. Fluorescent b.LED c. Laser d. UV

57._____ organization is essentially an array of selectively open and closed unidirectional contacts.

a.ROM b.RAM c. Computer d. All of the above

58.The EEPROM chip is physically similar to the chip.

a. EPROM b. Minterm c.POS d. Either a or b

59.A memory stores data for processing and the instructions for _____.

a. Result b. Execution c. Progress d.All of the above

60.Number of stored bits per unit area, which determines overall storage capacity and memory cost per bit.

a. Area Efficiency b. Access Time c. Power Consumption d. None of the above

61. The _____ of the desired memory location is applied to the address input terminals.

a. Name b. Address c. Number d. Level

62.In a sequential memory, the words are stored in and read out in a_____ .

a. Parallel b. Sequence c. Length d. None of the above

63.I/O function allows to exchange data directly between an

a. Process States b. Registers c. I/O module and the processor d.I/O device

64.Cache memory is intended to provide memory access

a. Fastest b. Slow c. Very Slow d. Fast

65.Data stores in_____

a. Monitor b. Mouse c. secondary storage d. Keyboard

66. Interrupts are provided primarily as a way to

a. Improve processor utilization b .Improve processor execution

c .Improve processor control d .Improve processor speed

67. Index register involves adding an

a. Index b. Instruction c. Information d. I/O device

68. Program counter contains the address of the

a. Next programs to be fetched b. Previous programs to be fetched

c. Previous information to be fetched d. Next information to be fetched

69. Memory modules consist of

a. Set of Instructions b. Set of Registers c. Set of Locations d. Set of Programs

70. Processor is often referred to

a. Central Processing Unit b. Hardware c. System Bus d. I/O Modules

71. I/O interrupt-driven is more efficient than

a. I/O Modules b. I/O Devices c. Programmed I/O d.CPU

72. Segment pointers divided memory into

a. Register b. Process c .Segments d. Scaling

73. The set of all logical addresses generated by a program is referred to as a

a. Memory Addresses b. Physical Addresses c. Logical address Space d. Buffer Addresses

74. The replacement algorithm chooses the constraints of

a. Blocks b. Cache Size c. Mapping Function d. Block Size

75.Data moved between computer components through

a.I/O Processor b. I/O Modules c. I/O Devices d. I/O Buffers

76. Condition codes are bits typically set by the

a. Processor execution b .processor operation c. Processor hardware d. Processor software

77. Instruction register contains the instructions most

a. recently deleted b. Recently fetched c. Recently updated d. Recently executed

78.The unit of data exchange between cache and main memory is known as

a. Cache Memory b. Cache Size c. Block Size d. Mapping Function

79.User-visible registers enable the machine or programmer to

a. Minimize Compiler b. Minimize Register c. Minimize Control d. Minimize Main Memory usage

80. Address registers contain main memory addresses of_____

A .Scheduling b. Registers c. Protocols d. Data and instruction

81. I/O instruction Control is used to activate an

a. Interrupt driven I/O b. Internal device c. External device d.I/O devices

82. I/O modules performs the requested action on

a. Programmed I/O b. Direct Memory Access (DMA) c. Interrupt driven I/O d. I/O devices

83. Control and Status registers used by the processor to control

a. Design of the Processor b. Operation of the Processor

c. Speed of the Processor d. Execution of the Processor

84.I/O instruction Transfer used to read the

a. Datab. Information c. Instructions d. Description

85. Stack pointer is a register that points to the

a. Pop the stack b. Push the stack c. Top of the stack d. Bottom of the stack

86.Cache size issue can have significant impact on

A. input b. output c. Information d. Performance

87. Direct memory access is more efficient to move

a. Less Data b. Large Data c. Largest Data d. Low Data

88. In data processing, processor perform some

a. Arithmetic or logic operation on information b. Arithmetic or logic operation on instruction

c. Arithmetic or logic operation on programs d. Arithmetic or logic operation on data

89. I/O instruction Status tests various

a. Control Conditions b. Status conditions c. I/O device d. Memory

90. The processor fetches an instruction from

a. Keyboard b. Monitor c. CPU d. Memory'+

91. Data and instructions that are being used frequently are stored in

a. Cache b. Block c. hard disk d. main memory

92. Processor-I/O involves data transferring between

a. Computers b. Processor and I/O modules c. Registers d. User Processes

93. Data register can be assigned to a

a. Variety of Functions b. Variety of Devices c. Variety of Programs d. Variety of systems

94. PerformanceX = 1/ Execution Time x the given relation shows that

a. Performance is increased when execution time is decreased

b. Performance is increased when execution time is increased

c. Performance is decreased when execution time is decreased d. None

95. The processor having Clock cycle of 0.25ns will have the clock rate of

a. 2GHz b. 3GHz c. 4GHz d. 8GHz

96. The valid and unimpeachable measurement of performance of any computer is

a. Clock rate b. Instruction set cExecution time d. Delay time

97. The native MIPS has the MIPS measurement of

a. MIPS = Instruction count/(Execution time)10^6

b. MIPS = Instruction count/(Execution time)10^3

c. MIPS = Instruction count/Execution time

d. MIPS = (Execution time)10^6

98. If computer A execute a program in 10 seconds and computer B runs the same in 15 seconds, how much faster is computer A than computer B

a. 1.4 times b. 1.5 times c. 1 time d. 5.1 times

99. For two computers X and Y, if the performance of computer X is greater than the performance of computer Y, we have

a. PerformanceX =2PerformanceX b. PerformanceX =PerformanceX

c. PerformanceX < PerformanceY d. PerformanceX > PerformanceY

100. The total amount of work done during execution, in a given time is referred to as

a. Response time b. Execution time c. Through put d. Delay time

ANSWERS:

51.c 52.b 53.b 54.d 55.c 56.d 57.a 58.a 59.d 60.a 61.b 62.b 63.c 64.a 65.c 6.a 67.a
68.d 69.c 70.a 71.c 72.c 73.c 74.c 75.b 76.c 77.b 78.c 79.d 80.d 81.c 82.a 83.b 84.a
85.c 86.d 87.b 88.d 89.b 90.d 91.b 92.b 93.a 94.a 95.c 96.c 97.a 98.b 99.d 100.c

101. To increase the performance of the computer its through put is increased by

a. Replacing processor with faster version b. Replacing input/output

c. Replacing Operating System d. Replacing Cache

102. Computer A having clock cycle time of 250 ps and cycle per instruction of 2.0 for some programs, and computer B having clock cycle time of 500 ps and a cycle per instruction of 1.2 for the same program. Which one is faster for this program

a. Computer A b. Computer B c. Both will have same time d. None of the above

103. When the PC having Clock rate of 2 and the CPU clock cycle for a program is 4 then Execution time of this computer for a program will be

a. 1 b. 1.5 c. 1.75 d. 2

104. The time between the start and the end of program execution is known as

a. Response time b. Execution time c. Delay time d. both a and b

105. A set of standard CPU-intensive, floating points and integers benchmarks are referred to as

a. SPEC benchmark b. PEC benchmark c. SEC benchmark d. SQEC benchmark

106. Computer B having execution time 110 ns and computer A having 1001 then

a. A is 9.1 times as fast as B for programs b. B is 9.1 times as fast as A for programs

c. A is 8 times as fast as B for programs d. B is 8 times as fast as A for programs

107. A first goal of compiler writer

a. Correctness b. Fast performance c. Callee saving d. Data dependence

108. Optimizations on the sources with output leading to later optimization passes are known as

a. Low-level optimizations b. High-level optimizations

c. Local optimizations d. Global optimizations

109. In 32-bit addressing mode, the address field is either 1 byte or

a. 2 bytes b. 3 bytes c. 4 bytes d. 5 bytes

110. The one of the advantage of MIPS 16 and Thumb is: the instruction caches acting as if they are about

a. 10% larger b. 25% larger c. 30% larger d. 40% larger

111. One of the complex jobs of the compiler writer, is to figure-out what instruction sequence will be used best for each segment, named as

a. Simplify trade-offs among alternatives b. Stack height reduction

c. Local optimizations d. Jumps

112. One that is used to allocate local variables is

a. Queue b. Stack c. Registers d. Banks

113. Vector architectures are operated on vectors of

a. Memory b. Data c.Registers d. Graph coloring

114. Graph coloring gives best results, when there are at-least

a. 16 general-purpose registers b. 24 general-purpose registers

c. 32 general-purpose registers d. 64 general-purpose registers

115. Compilers usually chooses which procedure calls has to be expanded inline before knowing the size of the procedure, that is being called, the stated problem is known as

a. Caller saving b. Callee saving c. Phase-ordering problem d. All above

116. The operation is normally specified in one field, known as

a. Oprand b. Opcode c. Operation d. Instruction count

117. The length of 80x86 instructions can vary between

a. 1 to 10 bytes b. 2 to 8 bytes c. 2 to 17 bytes d. 1 to 17 bytes

118. Optimization, known as basic block, by the compiler people is

a. Global common sub-expression elimination b. High-level optimizations

c. Local optimizations d. Global optimizations

119. The procedure when call procedure that has been called, saving the registers it wants for using, when the caller has been left unrestrained, is known as

a. Caller saving b. Calls c. Callee saving d. Jumps

120. When the call procedure saving the registers which it wants to be preserved to access even after the call, is refered to as

a. Caller saving b. Callee saving c. Calls d. Jumps

121. Replacing the instances of a variable, to which a constant is assigned with the constant, is refered as

a. Global common sub-expression elimination b. Stack height reduction

c. Heap d. Constant propagation

122. The optimization: finding two examples of an expression, computing the same value and saving the value of the 1st computation in a temporary variable, is refered as

a. Global common sub-expression elimination b. Global sub-expression elimination

c. Global elimination d. Sub-expression elimination

123. Register allocation algorithms are particularly based on the technique, named as

a. Low-level optimizations b. High-level optimizations

c. Phase-ordering problem d. Graph coloring

124. Specified telling that what addressing mode will be used for accessing the operand, is called

a. Address specified b. Binary-coded decimal c. Unpacking d. Packed decimal

125. Unit is used for allocating dynamic objects which do not adhere to the stack discipline is

a. Queue b. Stack c. Heap d. Banks

126. The developed program's performance, is affected by

a. Algorithm b. Compiler c. Operating system d. All above

127. The digital form of computer which is placed at the bank walls for dealing cash is known as

a. Automatic Teller Machine b. Super Computer c. Mini Computer d. Micro Computer

128. The modern supercomputers and the minicomputers, accessed by the network are called

a. Desktop Computers b. Laptops c. Servers d. Micro Computer

129. Every letter of the computer is referred to as

a. Bit b. Alphabet c. Nibble d. Number

130. Compiler of the system, is an example of

a. System hardware b. Input c. System software d. Output

131. Applications that are Consumer-Oriented embedded, are particularly best suited for

a. Multiprocessing b. Multitasking c. Many Functions d. One Function

132. The High level language, referred as human language, is converted into the computer instructions via

a. Compiler b. Interpreter c. Hardware system d. Software system

133. The programs which are used for translating the symbolic-language into the machine-language are

a. Compiler b. Assemblers c. Interpreters d. All above

134. Creating and translating the program, which one of the following is used

a. Software system b. Hardware system c. Compiler d. Interpreter

135. Microprocessors, that are present in home appliances are considered as the best example of

a. Desktop Computers b. Embedded Computers c. Servers d. Mini Computers

136. The layer which is between the system hardware and the user's program is commonly known as

a. Algorithm b. Network c. Operating system d. Functions

137. A+B in assembly language will be written as

a. add AB b. addition AB c. add A,B d. addition A,B

138. The information's components in base 2 are

a. 0 b. 1 c. integers d. both a and b

139. In assembly language A-B will be written as

a. sub AB b. subtraction AB c. sub A,B d. subtraction A,B

140. CPU provides enabling signals through

a. control bus b. data bus c. address bus d. ordinary bus

141. In a computer, set of electrical paths which is used to transfer data is called

a. bus b. monitors c. computer clock d. ports

142. Computer bus which allows the processor to communicate with peripheral devices is

a. expansion bus b. system bus c. memory bus d. processor bus

143. Computer address bus is

a. bidirectional b. unidirectional c. multidirectional d. circular

144. Computer bus with 64 lines can carry

a. 32bits b. 64bits c. 16bits d. 8bits

145. Which of the following is not a type of bus in computer?

a. data bus b. address bus c. timer bus d. control bus

146. Use of computer buses to connect different components of computer is known as

a. bus interconnection b. layout of computer components

c. computer structure d. bus topology

147. Network topology in which you connect each node to the network along a single piece of network cable is called

a. bus topology b. ring topology c. star topology d. mesh topology

148. Each end of a bus in computer bus network topology is termed as

a. node b. switch c. sensor d. terminator

149. Special resistor device in computer bus network topology which is attached to an electrical ground is called

a. terminato b. transistor c. switch d. sensor

150. Computer bus which moves data between the central processor and memory is called

a. I/O bu b. CPU bu S c. processor bu d. data bus

151. Type of computer bus which connects the CPU to a memory on the system board is

a. system bus b. word bus c. expansion bus d. width bus

152. Computer bus line is consists of

a. registers b. accumulators c. set of parallel lines d. computer clock

153. Way in which computer components are connected with each another is called

a. computer layout b. computer architecture c. computer parts d. computer hardware

154. Example of computer logic operation is

a. AND b. OR c. NOR d. all of these

155. Computer system mainly consists of

a. CPU b. main memory c. I/O unit d. all of these

156. Basic unit of computer is

a. ALU b. CU c. I/O unit d. all of these

157. Most of time, computer instructions are divided into

a. function code b. instruction code c. operand d. both a and c

158. Binary code which gives an actual instruction is called

a. instruction code b. logical code c. function code d. address

159. In instruction format, address of any data location is said to be

a. function code b. instruction code c. operand d. logical code

160. Built-in set of machine code instructions of computer are called

a. instruction set b. transfer of data c. logical operations d. logical set

161. Two main types of branch instructions are

a. conditional branch b. unconditional branch c. logical branch d. both a and b

162. Instructions that are programmed to make decisions are termed as

a. branch instructions b. programmed instructions

c. logical instructions d. arithmetic instructions

163. Branch instruction 'JUMP TO SUBORDINATE' is an example of

a. unconditional branch b. arithmetic branch c. transferring branch d. conditional branch

164. Branch instruction 'JUMP IF ZERO' is an example of

a. transferring branch b. conditional branch c. unconditional branch d. arithmetic branch

165. Branch instruction is also known as

a. jump instruction b. logical instruction c. arithmetic instruction d. programmed instructions

ANSWERS:

101.A 102.A 103.D 104.B 105.A 106.B 107.A 108.B 109.C 110.B 111.A 112.B 113.B
114.A 115.C 116.B 117.D 118.C 119.C 120.C 121.D 122.A 123.D 124.A 125.C 126.D
127.A 128.C 129.A 130.C 131.D 132.B 133.B 134.A 135.C 136.C 137.C 138.D 139.C
140.A 141.a 142.a 143.b 144.b 145.c 146.a 147.a 148.d 149.a 150.d 151.a 152.c 153.c
154.b 155.b 156.d 157.d 158.c 159.c 160.a 161.d 162.a 163.a 164.b 165.a

DIGITAL DATA REPRESENTATION

1. One byte equals to how many bits ?

a. 4 bits b. 8 bits c. 12 bits d. 16 bits

2. The numbers written to the power of 10 in the representation of decimal numbers are called as _____.

a. Height factors b. Size factors c. Scale factors d. None of the above

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3. If the decimal point is placed to the right of the first significant digit, then the number is called as _____.

a. Orthogonal b. Normalized c. Determinate d. None of the above

4. _____ constitute the representation of the floating number.

a. Sign b. Significant digits c. Scale factor d. All of the above

5. The sign followed by the string of digits is called as _____.

a. Significant b. Determinant c. Mantissa d. Exponent

6. In IEEE 32-bit representations, the mantissa of the fraction is said to occupy _____ bits.

a. 24 b. 23 c. 20 d. 16

7. The normalized representation of 0.0010110 * 2 ^ 9 is

a. 0 10001000 0010110 b. 0 10000101 0110

c. 0 10101010 1110 d. 0 11110100 11100

8. The 32 bit representation of the decimal number is called as ____.

a. Double-precision b. Single-precision c. Extended format d. None of the above

9. In 32 bit representation the scale factor as a range of _____.

a. -128 to 127 b. -256 to 255 c. 0 to 255 d. None of the above

10. In double precision format the size of the mantissa is _____.

a. 32 bit b. 52 bit c. 64 bit d. 72 bit

11. The 2's compliment of binary number 010111.1100 is

a. 101001.1100 b. 101000.0100 c. 010111.0011 d. 101000.0011

12. What is the 1's complement of 0000 1111 0010 1101 number?

a. 1111 0000 0010 1101 b. 1111 0000 1101 0010

c. 1111 1100 1010 11001 d. 1001 0010 1010 1100

13. The number of binary bits required to represent a hexadecimal digit is

a. 3 b. 4 c. 6 d. 8

14. A binary adder is a logic circuit that can add _____ binary numbers at a time.

a. Hundreds b. Thousands c. One d. Two

15. A 2's-complement adder-subtracter can add or subtract binary numbers. Sign-magnitude numbers represent _____ decimal numbers, and 2's complements stand for _____ decimal numbers.

a. hexa, sign b. sign, hexa c. positive, negative d. negative, positive

16. The main advantage of hexadecimal numbers is the case of conversion from hexadecimal to _____ and vice versa.

a. decimal b. binary c. ASCE d. BCD

17. A logic circuit which is used to change a BCD number into an equivalent decimal number is

a. decoder b. encoder c. multiplexer d. code converter

18. The digits used in a binary number system are _____ and _____.

a. 9 and 0 b. 0 and 1 c. 1 and 2 d. 3 and 4

19. The 1's compliment of binary number 11010 is:

a. 00101 b. 00010 c. 00110 d. 11101

20. The excess-3 code of decimal 7 is represented by

a. 1100 b. 1001 c. 1011 d. 1010

21. The conversation speed of an analog to digital converter is maximum with the following technique.

a. Dual slope AD converter. b. Serial comparator AD converter.

c. Successive approximation AD converter. d. Parallel comparator AD converter.

22. The ASCII code for letter A is

a. 1100011 b. 1000001 c. 1111111 d. 0010011

23. The negative numbers in the binary system can be represented by

a. Sign magnitude b. 1's complement c. 2's complement d. All of the above

24. Which of the following is a self complementing code?

a. 8421 code b. 5211 c. Gray code d. Binary code

25. Floating point representation is used to store

a. boolean values b. whole numbers c. real integers d. integers

26. Which of the following is not a weighted code?

a. Decimal Number system b. Excess 3-code c. Binary number System d. None of these

27. Which one is the possible technique for representing signed integers?

a. Signed Magnitude Representation b. Diminished Radix-Complement Representation

c. Radix-Complement Representation d. All of the above

28. What is used to represent the signed magnitude?

a. MSB b. LSB c. Both of the above d. None of the above

29. What are the two ways of representing the 0 with signed magnitude representation?

a. -0 and -0 b. +0 and +0 c. -0 and +0 d. None of the above

30. (FA)16 is the _____ one's complement representation of -5.

a. 4-bit b. 8-bit c. 16-bit d. 2-bit

31. 2's complement is used to represent signed integers, especially _____ integers.

a. Negative

b. Positive

c. Both a and b

d. None of the above

32. In _____, to encode a negative number, first the binary representation of its magnitude is taken, complement each bit and then add 1.

a. Signed integer representation

b. 1's complement representation

c. 2's complement representation

d. Radix complement representation

33. Which one of the following is the type of complement for each base R system?

a. Diminished radix-complement representation [(R – 1)'s complement]

b. Radix- complement representation [R's complement]

c. 1's and 2's complement representation

d. Both a and b

34. For subtraction of binary number, subtract the _____.

a. Minuend from the subtrahend digit

b. Subtrahend digit from the minuend

c. MSB from the LSB

d. None of the above

35. Which of the following condition is true for determining overflow condition in 2's complement?

a. When adding two positive numbers gives a negative result or when two negatives give a positive result

b. If sign bit (MSB) of result and sign bit of two operands are of different signs.

c. The '1' in the MSB position indicates a negative number after adding two positive numbers.

d. All of the above

36. What does the leftmost bit represents, according to the IEEE standards?

a. Sign of the number b. Position of the number c. Weight of the number d. None of the above

37. Floating-point numbers are those numbers, which include _____.

a. Decimals b. Fractional parts c. Integer values d. All of the above

38. The binary representation of 0.875 is 0 01111110 11000000000000000000000 in _____presentation.

a. 128- bit b. Excess 127 c. 32- bit d. 16-bit

39. 1000001 represents as (65)10 in which code?

a. ASCII code b. Straight binary code c. Gray code d. BCD code

40. In straight binary code, N-bits or N binary digits can represent _____ different values.

a. 2^N b. 2^(N+1) c. 2^(N-1) d. 2^N -1

41. Which of the following code is also known as reflected code?

a. Excess-3 code

b. Gray code

c. Straight binary code

d. Error code

a. MSB to the next bit

b. LSB to the next bit

c. MSB of the previous bit

d. LSB of the previous bit

43. ASCII code is required for representing more than _____ characters.

a. 16

b. 8

c. 64

d. 32

44. Why the 8-bit (MSB) is added in EBCDIC?

a. For carriage return

b. For making the total number of 1’s odd

c. For line feed

d. For parity

45. What is the 8-bit EBCDIC representation of alphabet M?

a. 1100100

b. 11001001

c. 11010100

d. 010001

46. Which of the following is not correct regarding EBCDIC?

a. It is used to represent more than 64 characters.

b. It is a 7-bit code.

c. A maximum of 128 different characters can be represented by this code.

d. None of the above

47. The MSB of _____ is same as the MSB of the corresponding Gray code.

a. Alphanumeric code

b. Excess-3 code

c. Binary code

d. Gray code

48. How can you represent (08)10 in BCD?

a. 0000 1000

b. 0010 0011

c. 1001 0010 0001

d. 1001 0010

49. In N-bits, you can represent the signed integers ranging from _____.

a. 2 ^(N-1) to 2^ (N+1)

b. -2^(N-1) to 2^(N-1) -1

c. 2 ^(N+1) to 2^(N-1) +1

d. 2^ (N) to 2^ (N+1)

50. How -5 is represented in hex format in 2’s complement in 8-bits?

a. (FB)16 b. (7F)16 c. (FF)16 d. (FA)16

ANSWERS:

1.B 2.C 3.B 4.D 5.C 6.B 7.B 8.B 9.A 10.B 11.B 12.B 13.B 14.D 15.C 16.B 17.A 18.B 19.A 20.C 21.D 22.B 23.C 24.A 25.C 26.B 27.D 28.A 29.C 30.B 31.A 32.C 33.D 34.B 35.B 36.A 37.D 38.C 39.B 40.A 41.B 42.A 43.C 44.D 45.C 46.B 47.C 48.A 49.B 50.A

51. What is the 9's complement of (0.3267)10?

a. 47.479 b. 0.6352 c. 0.6732 d. 1.4563

52. How can you represent = in 8-bit EBCDIC representation?

a. 01111111 b. 01111110 c. 01011100 d. 01101011

53. Boolean algebra is named after_____, who used it to study human logical reasoning.

a. Anderson, Mary b. Acharya Kanad c. Dickson, Earle d. George Boole

54. BCD code is

a. non-weighted b. the same thing as binary numbers

c. a binary code d. an alphanumeric code

55. Resultant binary of the decimal problem 49 + 1 is

a. 00110010 b. 110011 c. 1010101 d. 111100

56. The number of bits used to store a BCD digit is

a. 2 b. 4 c. 6 d. 8

57. In Excess-3 code each coded number is

a. four larger than in BCD code b. three smaller than in BCD code

c. three larger than in BCD code d. much larger than in BCD code

58. Binary equivalent of A16 is

a. 1010 b. 1011 c. 1000 d. 1110

59. All of the following are 4-bit combinations of BCD code except

a. 1010 b. 1100 c. 1000 d. 1001

60. Data keys need not be a direct hardware address in

a. hard disk b. memory c. RAM d. ROM

61. Binary files are sometimes referred as

a. data b. information c. instruction d. command

62. Digital data is represented using

a. binary system b. alphabetic system c. processing system d. numeric system

63. Data can be organized in many different types of data structures, including

a. arrays b. graphs c. objects d. all of these

64. To store data bytes in a file, they have to be serialized in a

a. file format b. data format c. binary format d. numeric format

65. To convert a whole decimal number into a hexadecimal equivalent, one should divide the decimal value by

a. 2 b. 8 c. 10 d. 16

66. Hexadecimal number system is used as a shorthand language to represent

a. decimal numbers b. binary numbers c. octal numbers d. quinary numbers

67. Numbering system which uses numbers and letters as symbols is termed as

a. decimal b. binary c. octal d. hexadecimal

68. Convert the binary number 1011010 to hexadecimal

a. 5C b. 5A c. 5F d. 5B

ANSWERS:

51.C 52.B 53.D 54.C 55.A 56.B 57.C 58.A 59.A 60.B 61.A 62.A 63.D 64.A 65.A 66.A 67.D 68.B

BASIC COMPUTER ORGANIZATION

1. The main virtue for using single Bus structure is

a. Fast data transfers b. Cost effective connectivity and speed

c. Cost effective connectivity and ease of attaching peripheral devices d. None of these

2. _____ are used to over come the difference in data transfer speeds of various devices.

a. Speed enhancing circuitory b. Bridge circuits c. Multiple Buses d. Buffer registers

3. To extend the connectivity of the processor bus we use _____ .

a. PCI bus b. SCSI bus c.Controllers d. Multiple bus

4. IBM developed a bus standard for their line of computers 'PC AT' called _____ .

a. IB bus b. M-bus c. ISA d. None of these

5. The bus used to connect the monitor to the CPU is _____ .

a. PCI bus b. SCSI bus c. Memory bus d. Rambus

6. ANSI stands for

a. American National Standards Institute

b. American National Standard Interface

c. American Network Standard Interfacing

d. American Network Security Interrupt

7. _____ register Connected to the Processor bus is a single-way transfer capable.

a. PC

b. IR

c. Temp

d. Z

8. In multiple Bus organisation, the registers are collectively placed and referred as _____ .

a. Set registers

b. Register file

c. Register Block

d. Map registers

9. The main advantage of multiple bus organisation over single bus is

a. Reduction in the number of cycles for execution

b. Increase in size of the registers

c. Better Connectivity

d. None of these

10. The ISA standard Buses are used to connect

a. RAM and processor

b. GPU and processor

c. Harddisk and Processor

d. CD/DVD drives and Processor

ANSWERS:

1.C 2.D 3.A 4.C 5.B 6.A 7.D 8.B 9.B 10.C

11. Which of the following is not a form of memory ?

a. Instruction cache

b. Instruction register

c. Instruction opcode

d. Both a and b

Answer: (c).

12. Which memory is difficult to interface with processor ?

a. Static memory

b. Dynamic memory

c. ROM

d. None of these

Answer: (b).

13. Desirable characteristic(s) of a memory system is(are)

a. Speed and reliability

b. Low power consumption

c. Durability and compactness

d. All of these

Answer: (d).

14. The minimum time delay required between initiation of two successive memory operations is called

a. Memory cycle time

b. Memory access time

c. Transmission time

d. Fetch Time

Answer: (a).

15. For a memory system, the cycle time is

a. Same as the access time

b. Longer than the access time

c. Shorter than the access time

d. multiple of the access time

Answer: (b).

16. Generally , the refreshing rate of dynamic RAMs is approximately once in

a. Two micro seconds

b. Two milli seconds

c. Sixty four milli seconds

d. Two micro seconds

Answer: (b).

17. In comparison with static RAM memory, the dynamic RAM memory has

a. Lower bit density and higher power consumption

b. Higher bit density and low power consumption

c. Lower bit density and lower power consumption

d. None of these

Answer: (b).

18. Disadvantage of dynamic RAM over static RAM is

a. Higher power consumption

b. Variable speed

c. Need to refresh the capacitor charge every once in two milliseconds

d. Lower Packing density

Answer: (c).

19. Memory consisting of electronic circuits attached into silicon chip is known as

a. Magnetic core memory

b. Semiconductor memory

c. Thin film memory

d. None of these

Answer: (b).

20. Which of the following is the internal memory of the system (computer) ?

a. CPU register

b. Cache

c. Main memory

d. All of these

Answer: (d).

21. The idea of cache memory is based on

a. The property of locality of reference

b. The heuristic 90-10 rule

c. The fact that only a small portion of a program is referenced relatively frequently

d. None of these

Answer: (a).

22. What is the correct sequence of time delays that happen during a data transfer from a disk to memory?

a. Seek time, access time, transfer time

b. Seek time, latency time, transfer time

c. Access time ,Latency time, transfer time

d. Latency time, access time, transfer time

Answer: (b).

23. An 24 bit address generates an address space of _____ locations .

a. 1024

b. 4096

c. 2 ^ 48

d. 16,777,216

Answer: (d).

24. If a system is 64 bit machine , then the length of each word will be ____ .

a. 4 bytes

b. 8 bytes

c. 16 bytes

d. 12 bytes

Answer: (b).

25. The type of memory assignment used in Intel processors is _____ .

a. Little Endian

b. Big Endian

c. Medium Endian

d. None of the above

Answer: (a).

26. When using the Big Endian assignment to store a number, the sign bit of the number is stored in _____ .

a. The higher order byte of the word

b. The lower order byte of the word

c. Can’t say

d. None of the above

Answer: (a).

27. To get the physical address from the logical address generated by CPU we use ____ .

a. MAR

b. MMU

c. Overlays

d. TLB

Answer: (b).

28. _____ method is used to map logical addresses of variable length onto physical memory.

a. Paging

b. Overlays

c. Segmentation

d. Paging with segmentation

Answer: (c).

29. During transfer of data between the processor and memory we use _____ .

a. Cache

b. TLB

c. Buffers

d. Registers

Answer: (d).

30. Physical memory is divided into sets of finite size called as _____ .

a. Frames

b. Pages

c. Blocks

d. Vectors

Answer: (a).

31. Which is true for a typical RISC architecture?

a. Micro programmed control unit

b. Instruction takes multiple clock cycles

c. Have few registers in CPU

d. Emphasis on optimizing instruction pipelines

Answer: (a).

32. SIMD represents an organization that _____.

a. refers to a computer system capable of processing several programs at the same time.

b. represents organization of single computer containing a control unit, processor unit and a memory unit.

c. includes many processing units under the supervision of a common control unit.

d. none of the above

Answer: (c).

33. Suppose that a bus has 16 data lines and requires 4 cycles of 250 nsecs each to transfer data. The bandwidth of this bus would be 2 Megabytes/sec. If the cycle time of the bus was reduced to 125 nsecs and the number of cycles required for transfer stayed the same what would the bandwidth of the bus?

a. 1 Megabyte/sec

b. 4 Megabytes/sec

c. 8 Megabytes/sec

d. 2 Megabytes/sec

Answer: (d).

34. Von Neumann architecture is

a. SISD

b. SIMD

c. MIMD

d. MISD

Answer: (a).

35. A Stack-organised Computer uses instruction of

a. Indirect addressing

b. Two-addressing

c. Zero addressing

d. Index addressing

Answer: (c).

36. An n-bit microprocessor has

a. n-bit program counter

b. n-bit address register

c. n-bit ALU

d. n-bit instruction register

Answer: (d).

37. PSW is saved in stack when there is a

a. interrupt recognised

b. execution of RST instruction

c. execution of CALL instruction

d. All of these

Answer: (a).

38. _____ register keeps tracks of the instructions stored in program stored in memory.

a. AR (Address Register)

b. XR (Index Register)

c. PC (Program Counter)

d. AC (Accumulator)

Answer: (c).

39. 'Aging registers' are

a. Counters which indicate how long ago their associated pages have been referenced.

b. Registers which keep track of when the program was last accessed.

c. Counters to keep track of last accessed instruction.

d. Counters to keep track of the latest data structures referred.

Answer: (a).

40. Translation from symbolic program into Binary is done in

a. Two passes

b. Directly

c. Three passes

d. Four passes

Answer: (a).

41. MIMD stands for

a. Multiple instruction multiple data

b. Multiple instruction memory data

c. Memory instruction multiple data

d. Multiple information memory data

Answer: (a).

42. A k-bit field can specify any one of

a. 3^k registers

b. 2^k registers

c. K^2 registers

d. K^3 registers

Answer: (b).

43. The time interval between adjacent bits is called the

a. Word-time

b. Bit-time

c. Turn around time

d. Slice time

Answer: (b).

44. The communication between the components in a microcomputer takes place via the address and

a. I/O bus

b. Data bus

c. Address bus

d. Control lines

Answer: (b).

45. Data input command is just the opposite of a

a. Test command

b. Control command

c. Data output

d. Data channel

Answer: (c).

46. A binary digit is called a

a. Bit

b. Byte

c. Number

d. Character

Answer: (a).

47. An interface that provides a method for transferring binary information between internal storage and external devices is called

a. I/O interface

b. Input interface

c. Output interface

d. I/O bus

Answer: (a).

48. An address in main memory is called

a. Physical address

b. Logical address

c. Memory address

d. Word address

Answer: (a).

49. The information available in a state table may be represented graphically in a

a. simple diagram

b. state diagram

c. complex diagram

d. data flow diagram

Answer: (b).

50. An interface that provides I/O transfer of data directly to and form the memory unit and peripheral is termed as

a. DDA

b. Serial interface

c. nBR

d. DMA

Answer: (d).

51. A register capable of shifting its binary information either to the right or the left is called a

a. parallel register

b. serial register

c. shift register

d. storage register

Answer: (c).

52. Which of the following is a main memory?

a. Secondary memory

b. Auxiliary memory

c. Cache memory

d. Virtual memory

Answer: (c).

53. The maximum addressing capacity of a micro processor which uses 16 bit database & 32 bit address base is

a. 64 K

b. 4 GB

c. Both a and b

d. None of these

Answer: (b)

54. A successive A/D converter is

a. a high-speed converter

b. a low speed converter

c. a medium speed converter

d. none of these

Answer: (c).

55. A stack organized computer has

a. Three-address Instruction

b. Two-address Instruction

c. One-address Instruction

d. Zero-address Instruction

Answer: (d).

56. A Program Counter contains a number 825 and address part of the instruction contains the number 24. The effective address in the relative address mode, when an instruction is read from the memory is

a. 849

b. 850

c. 801

d. 802

Answer: (b).

57. A system program that translates and executes an instruction simultaneously is

a. Compiler

b. Interpreter

c. Assembler

d. Operating system

Answer: (c).

58. The memory location's address where data is to be stored is specified by _____.

a. Memory Buffer Register (MBR)

b. Accumulator (AC)

c. Instruction Register (IR)

d. Memory Address Register (MAR)

Answer: (d).

59. The number of instructions being executed defines the

a. Instruction count

b. Hit time

c. Clock rate

d. All above

Answer: (a).

60. Energy equation of pulse of the logic transition, can be computed as

a. Energydynamic ? Capacitive load

b. Energydynamic 1/? Capacitive load

c. Energydynamic ? Capacitive load - Voltage2

d.nEnergydynamic ? Capacitive load + Voltage2

Answer: (a).

61. Software compatibility levels determines

a. Amount of existing software

b. Flexibility

c. Protection

d. Networking

Answer: (a).

62. The no of good dies/wafer are called

a. Top line

b. Bottom line

c. Double line

d. Multiple line

Answer: (b).

63. 3.3 GHz Core i7 running in short bursts for

a. 1.6 GHz

b. 3.3 GHz

c. 3.6 GHz

d. 2.6 GHz

Answer: (c)

64. 80% cost of a $90M warehouse is associated with,

a. Power

b. Cooling

c. Scaling

d. both a and b

Answer: (d).

65. The no of dies/300 mm or (30 cm)wafer for die which is 1.5 cm on a side and for that die which is 1.0 cm on a side, would be

a. 370 & 640

b. 270 & 740

c. 270 & 750

d. 270 & 640

Answer: (d).

66. For comparing the performance of new system, the users will simply compare execution time of its

a. Response time

b. Execution time

c. Workloads

d. Multitasking

Answer: (c).

67. With respect to changing among the states of accomplishment and interruption, a measure of continuous service-accomplishment, is known as

a. Module availability

b. Scalability

c. Module reliability

d. Sector

Answer: (a).

68. Sustained power consumption; the given metric is widely known as

a. Thermal design power

b. Electrical design power

c. Hydro design power

d. None of above

Answer: (a).

69. Databases and transaction processing support; reliability and availability enhancements are provided by

a. Desktop

b. Clusters

c. Servers

d. Tabs

Answer: (c).

70. Static power being directly proportional to no of devices, that is known as

a. Powerstatic ? Currentstatic

b. Powerstatic ? Currentstatic + Voltage

c. Powerstatic ? Currentstatic - Voltage

d. Powerstatic ? Currentstatic Voltage

Answer: (a).

71. 15% reduction in voltage results in a 15% frequency reduction, the impact on the dynamic energy and the dynamic power, is

a. 0.82

b. 0.12

c. 0.78

d. 0.61

Answer: (d).

72. The most common and simple definition of time is called

a. Wall-clock time

b. Response time

c. Elapsed time

d. All above

Answer: (d).

73. Every easily made mistakes and flaws in the computer design and architecture, are referred to as

a. Fallacies

b. Pitfalls

c. Error

d. Debugging

Answer: (b).

74. The sound output has data-rate of approximately

a. 4

b. 6

c. 7

d. 8

Answer: (d).

75. 1000 disks having 1,000,000-hour MTTF, if failed disks are being replaced with a new one, having the same as all having reliability characteristics, the number of disks that would be failed in a year (8760 hours) is

a. 4

b. 8

c. 9

d. 12

Answer: (c).

76. Dies which are 1.5cm on a side and 1.0cm on a side, supposing a density of 0.031/per cm^2 and N is 13.5, will have die yielding

a. 0.4 and 0.66

b. 0.4 and 1.66

c. 1.4 and 0.66

d. 2.4 and 0.66

Answer: (a).

77. By improving the components of the computer for the performance gain, can be calculated using

a. Ampere's law

b. Bottom line

c. Module reliability

d. Amdahl

Answer: (d).

78. The largest form of the clusters are called

a. Warehouse-scale computers

b. Data center

c. Scaling computers

d. Supercomputers

Answer: (a).

79. Different types of parallelism in the applications like:

a. Data-Level Parallelism

b. Task-Level Parallelism

c. Instruction-Level Parallelism

d. All above

Answer: (d).

80. Benchmarks remain indefinitely valid, the given statement is referred to as

a. Fallacy

b. Pitfall

c. Debug

d. mError

Answer: (a).

81. Single instruction single data stream (SISD) category is the

a. Uniprocessor category

b. Dualprocessor category

c. Quadcore category

d. Multipleprocessor

Answer: (a).

82. For measuring the ability of a computer system for handling the transactions that is consisted of access of database and updates of benchmark used is

a. Server Benchmarks

b. Desktop Benchmarks

c. Synthetic benchmarks,

d. Transaction-processing (TP) benchmarks

Answer: (d).

83. The term 'computer architecture' is sometimes referred only to

a. Instruction set design

b. Circuit design

c. Hardware design

d. Pipelining

Answer: (a).

84. Thousands of concentric circles, magnetic-disk are made up of are known as

a. Tracks

b. Sectors

c. Files

d. Surface

Answer: (a).

85. The general categories of instructions' operation are

a. Data transfer

b. Arithmetic logical

c. floating point

d. All above

Answer: (d).

86. A wafer is normally tested and is chopped into

a. Dies

b. Tri

c. Tabs

d. Tracks

Answer: (a).

87. Programs which are tend to reusing data as well as instructions they have used just before, is known as

a. Principle of locality

b. Temporal locality

c. Spatial locality

d. Scalability

Answer: (a).

88. Being able for expanding memory, no of processors and the disks is called

a. Durability

b. Scalability

c. Synthetic

d. Production

Answer: (b).

89. SaaS is known as a growing software as a

a. System

b. Set

c. Service

d. Sector

Answer: (c).

90. From a reference initial instant, a measure of service accomplishment. is known as

a. Hardware

b. Scalability

c. Module reliability

d. Sector

Answer: (c).

91. The cost of the die can be calculated as

a. Cost of die= Cost of wafer Dies per wafer + Die yield

b. Cost of die= Cost of wafer Dies per wafer - Die yield

c. Cost of die= Cost of wafer Dies per wafer

d. Cost of die= Cost of wafer Dies per wafer Die yield

Answer: (c).

92. Fake programs that are made to try to compare the profile and behavior of original applications, such as Dhrystone are called as

a. Synthetic benchmarks

b. Kernel

c. Toy programs

d. None of above

Answer: (a).

93. Data-level parallelism/task-level parallelism in a tightly coupled hardware which allows interaction among parallel threads, are processed by

a. Instruction-Level Parallelism

b. Request-Level Parallelism

c. Thread-Level Parallelism

d. Vector Architectures and Graphic Processor Units

Answer: (c).

94. The no of dies/wafer is approximately the area of wafer which is divided by the area of this die. It is estimated by

a. (? (Wafer diameter/2)2Die area)+(?

b. (? (Wafer diameter/2)2Die area)-(?

c. (? (Wafer diameter/2)2Die area)*(?

d. (? (Wafer diameter/2)2Die area)(?

Answer: (b).

95. In switching transistors the traditional primary energy-consumption, also called

a. Static energy

b. Dynamic energy

c. Mechanical energy

d. Thermal energy

Answer: (b).

96. Power is energy/unit time: 1 watt =

a. 1 coulomb per second

b. 1 joule per second

c. 1 joule

d. 1second

Answer: (b).

97. Desktop benchmarks; which are divided into a

a. Single broad class

b. Two broad classes

c. Three broad classes

d. Four broad classes

Answer: (b).

98. MISD data stream is the abbreviation of

a. Multiple instruction single data stream

b. Multiple instruction streams, single data stream

c. Multiple instruction streams, data stream

d. Many instruction streams, single data stream

Answer: (b).

99. A time between the start and accomplishment of an event, is called a

a. Response time

b. Execution time

c. Delay time

d. both a and b

Answer: (d).

100. A 2nd key feature of server systems is

a. Performance

b. Scalability

c. Price reduction

d. Computation

101. Reporting performance measurements' guiding principle would be
a. Durability
b. Scalability
c. Reproducibility
d. None of above
Answer: (c).

102. If floating-point instructions are not being executed, then the floating-point unit will have a clock of
a. Enabled
b. Disabled
c. Continues
d. No effect
Answer: (b).

103. Processor A having 20% higher power-consumption than the processor B, but if processorA executes task in only 70% of average time needed by B, then its energy consumption will be
a. 0.81
b. 0.94
c. 0.84
d. 0.91
Answer: (c).

104. Products being sold by multiple vendors in very large number are called
a. Thermal design power

b. Clusters
c. Servers
d. Commodities
Answer: (d).
105. The response time matters in the commercial market, uses like:
a. web servers
b. Tracking systems
c. Atms
d. All above
Answer: (d).
106. Transistor density increasing by 35%/year, quadrupling over the 4years, the given technology is known as
a. Integrated logic technology
b. Multi circuit logic technology
c. Multi instruction logic technology
d. Integrated circuit logic technology
Answer: (d).
107. In floating point instruction format the Opcode contains
a. 25-32 bits
b. 26-31 bits
c. 24-31 bits
d. 26-32 bits
Answer: (b).
108. Size of computer accumulator register can be of
a. 4 bit
b. 4 KB
c. 4 bytes
d. 4 Mbytes
Answer: (c).
109. Computer component which is fastest is
a. RAM
b. cache
c. register
d. hard disk
Answer: (c).
110. In computer, size of DI, SI, SP and BP stack control register is
a. 2 bytes each
b. 6 bytes each
c. 4 bytes each
d. 8 bytes each
Answer: (a).
111. Register used as a working area in CPU is
a. program counter
b. instruction register

c. instruction decoder
d. accumulator
Answer: (d).
112. Fetch operation are not required in
a. direct addressing
b. indirect addressing
c. immediate addressing
d. register addressing
Answer: (c).
113. Example of implied addressing is
a. stack addressing
b. immediate addressing
c. indirect addressing
d. direct addressing
Answer: (a).
114. Which of the following is not a kind of register?
a. flag
b. segment
c. accumulator
d. math coprocessor
Answer: (d).
115. In an instruction, address part points to the address of the actual data, than the address mode is
a. immediate addressing
b. direct addressing
c. indirect addressing
d. stack addressing
Answer: (b)
116. Addressing mode used in the instruction PUSH B, is
a. direct
b. indirect
c. immediate
d. register
Answer: (c).
117. Immediate addressing mode of instruction provides the operand in the memory location to
a. pointed by the PC
b. next of OP code
c. pointed by PC+1
d. pointed by PC+2
Answer: (b).
118. Addressing mode used in an instruction of the form ADD X, Y, is
a. absolute
b. immediate
c. indirect

d. index
Answer: (a).
119. Which of the following is not the type of computer register?
a. address registers
b. accumulators
c. general-purpose registers
d. all are types of registers
Answer: (d).
120. Component used to store one or more bit of data and can accept and/or transfer information serially is called
a. parallel registers
b. shift registers
c. counters
d. data registers
Answer: (b).
121. Computer register which collects the result of computation is called
a. instruction pointer
b. storage
c. storage register
d. accumulator
Answer: (d).

122. Temporary storage area within CPU is called
a. register
b. ROM
c. RAM
d. ALU
Answer: (a).
123. In register addressing mode operands are looked in
a. cache
b. secondary storage
c. CPU
d. primary memory
Answer: (c).
124. Computer register which is used to keep track of address of the memory location where the next instruction is located is
a. memory address register
b. memory data register
c. instruction register
d. program counter
125. In the indirect address mode,
a. effective address is equal to address part of instruction
b. content of program counter is added to address part of instruction
c. a memory is addressed by a register

d. address in the instruction points to location of effective address
Answer: (c).

INPUT OUTPUT ORGANIZATION

1. In memory-mapped I/O…
a.The I/O devices and the memory share the same address space
b.The I/O devices have a seperate address space
c. The memory and I/O devices have an associated address space
d. A part of the memory is specifically set aside for the I/O operation
Answer: (a).
2. The usual BUS structure used to connect the I/O devices is
a. Star BUS structure
b. Multiple BUS structure
c. Single BUS structure
d. Node to Node BUS structure
Answer: (c).
3. The advantage of I/O mapped devices to memory mapped is
a. The former offers faster transfer of data
b. The devices connected using I/O mapping have a bigger buffer space
c. The devices have to deal with fewer address lines
d. No advantage as such
Answer: (c).
4. The system is notified of a read or write operation by
a. Appending an extra bit of the address
b. Enabling the read or write bits of the devices
c. Raising an appropriate interrupt signal
d. Sending a special signal along the BUS
Answer: (d).
5. To overcome the lag in the operating speeds of the I/O device and the processor we use
a. Buffer spaces
b. Status flags
c. Interrupt signals
d. Exceptions
Answer: (b).
6. The method of accessing the I/O devices by repeatedly checking the status flags is
a. Program-controlled I/O
b. Memory-mapped I/O
c. I/O mapped
d. None of the above
Answer: (a).
7. The method of synchronising the processor with the I/O device in which the device sends a signal when it is ready is
a. Exceptions
b. Signal handling

c. Interrupts
d.DMA
Answer: (c).
8. The method which offers higher speeds of I/O transfers is
a. Interrupts
b. Memory mapping
c. Program-controlled I/O
d.DMA
Answer: (d).
9. The process where in the processor constantly checks the status flags is called as
a. Polling
b. Inspection
c. Reviewing
d. Echoing
Answer: (a).
10.The interrupt-request line is a part of the
a. Data line
b. Control line
c. Address line
d. None of the above
Answer: (b).
11.The return address from the interrupt-service routine is stored on the
a. System heap
b. Processor register
c. Processor stack
d. Memory
Answer: (c).
12. The signal sent to the device from the processor to the device after recieving an interrupt is
a. Interrupt-acknowledge
b. Return signal
c. Service signal
d. Permission signal
Answer: (a).
13. When the process is returned after an interrupt service _____ should be loaded again
i) Register contents
ii) Condition codes
iii) Stack contents
iv) Return addresses
a. i,iv
b. ii,iii and iv
c. iii,iv
d. i,ii
Answer: (d).
14. The time between the receive of an interrupt and its service is _____

a. Interrupt delay
b. Interrupt latency
c. Cycle time
d. Switching time
Answer: (b).
15. Interrupts form an important part of _____ systems.
a. Batch processing
b. Multitasking
c. Real-time processing
d. Multi-user
Answer: (c).
16. _____ type circuits are generally used for interrupt service lines
i) open-collector
ii) open-drain
iii) XOR
iv) XNOR
a. i,ii
b. ii
c. ii,iii
d. ii,iv
Answer: (a).
17. The resistor which is attached to the service line is called _____.
a. Push-down resistor
b. Pull-up resistor
c. Break down resistor
d. Line resistor
Answer: (b).
18. An interrupt that can be temporarily ignored is
a. Vectored interrupt
b. Non-maskable interrupt
c. Maskable interrupt
d. High priority interrupt
Answer: (c).
19. The 8085 microprocessor respond to the presence of an interrupt
a. As soon as the trap pin becomes 'LOW'
b. By checking the trap pin for 'high' status at the end of each instruction fetch
c. By checking the trap pin for 'high' status at the end of execution of each instruction
d. By checking the trap pin for 'high' status at regular intervals
Answer: (c).
20. CPU as two modes privileged and non-privileged. In order to change the mode from privileged to non-privileged
a. A hardware interrupt is needed
b. A software interrupt is needec.Either a or b
d. A non-privileged instruction (which does not generate an interrupt)is needed

Answer: (b).
21. Which interrupt is unmaskable…??
a. RST 5.5
b. RST 7.5
c. TRAP
d. Both a and b
Answer: (c).
22. From amongst the following given scenarios determine the right one to justify interrupt mode of data transfer
i) Bulk transfer of several kilo-byte
ii) Moderately large data transfer of more than 1kb
iii) Short events like mouse action
iv) Keyboard inputs
a. i and ii
b. ii
c. i,ii and iv
d. iv
Answer: (d).
23. How can the processor ignore other interrupts when it is servicing one
a. By turning off the interrupt request line
b. By disabling the devices from sending the interrupts
c. By using edge-triggered request lines
d. All of the above
Answer: (d).
24. When dealing with multiple device interrupts , which mechanism is easy to implement
a. Polling method
b. Vectored interrupts
c. Interrupt nesting
d. None of the above
Answer: (a).
25. The interrupt servicing mechanism in which the reqesting device identifies itself to the processor to be serviced is
a. Polling
b. Vectored interrupts
c. Interrupt nesting
d. Simultaneous requesting
Answer: (b).
26. Which table handle stores the addresses of the interrupt handling sub-routines
a. Interrupt-vector table
b. Vector table
c. Symbol link table
d. None of these
Answer: (a).
27. Interrupts initiated by an instruction is called as

a. Internal
b. External
c. Hardware
d. Software
Answer: (b).
28. The anded output of the bits of the interrupt register and the mask register are set as input of:
a. Priority decoder
b. Priority encoder
c. Process id encoder
d. Multiplexer
Answer: (b).
29. ____ register is used for the purpose of controlling the status of each interrupt request in parallel priority interrupt.
a. Mass
b. Mark
c. Make
d. Mask
Answer: (d).
30. _____ interrupt method uses register whose bits are set separately by interrupt signal for each device:
a. Parallel priority interrupt
b. Serial priority interrupt
c. Daisy chaining
d. None of the above
Answer: (a).
31. In daisy chaining device 0 will pass the signal only if it has..
a. Interrupt request
b. No interrupt request
c. Both a and b
d. None of the above
Answer: (b).
32. _____ method is used to establish priority by serially connecting all devices that request an interrupt.
a. Vectored-interrupting
b. Daisy chain
c. Priority
d. Polling
Answer: (b).
33. Which one of the following is true with regard to a CPU having a single interrupt request line and single interrupt grant line…??
i) Neither vectored nor multiple interrupting devices is possible.
ii) Vectored interrupts is not possible but multiple interrupting devices is possible.
iii) Vectored interrupts is possible and multiple interrupting devices is not possible.

iv) Both vectored and multiple interrupting devices is possible.
a. iii
b. i,iv
c. ii,iii
d. iii,iv
Answer: (a).
34. The processor indicates to the devices that it is ready to recieve interrupts
a. By enabling the interrupt request line
b. By enabling the IRQ bits
c. By activating the interrupt acknowledge line
d. Either a or b
Answer: (c).
35. The starting address sent by the device in vectored interrupt is called as
a. Location id
b. Interrupt vector
c. Service location
d. Service id
Answer: (b).
36. The code sent by the device in vectored interrupt is _____ long.
a. upto 16 bits
b. upto 32 bits
c. upto 24 bits
d. 4-8 bits
Answer: (d).
37. In vectored interrupts, how does the device identify itself to the processor..?
a. By sending its device id
b. By sending the machine code for the interrupt service routine
c. By sending the starting address of the service routine
d. Either a or c
Answer: (c).
38. DMA interface unit eliminates the need to use CPU registers to transfer data from
a. MAR to MBR
b. MBR to MAR
c. I/O units to memory
d. Memory to I/O units
Answer: (d).
39. The average time required to reach a storage location in memory and obtain its contents is called the
a. seek time
b. turnaround time
c. access time
d. transfer time
Answer: (c).
40. The process that periodically checks the status of an I/O devices, is known as

a. Cold swapping
b. I/O instructions
c. Polling
d. Dealing
Answer: (c).
41. A bus connecting processor and memory, is known as
a. Processor-memory bus
b. Bus transaction
c. Backplane bus
d. Synchronous bus
Answer: (a).
42. 1000 disks having 1,200,000-hour MTTF and disks being used 24 hours a day, and failed disks are being replaced with a new ones, then no that will fail over five years (43,800 hours) is,
a. 25
b. 30
c. 36
d. 40
Answer: (c).
43. A unit on the bus that initiates bus requests is called
a. Slave
b. Controller master
c. Striping
d. Bus master
Answer: (d).
44. Request, which is used for indicating a read request for memory, is known as
a. ReadReq
b. WriteReq
c. DataReq
d. Hot swapping
Answer: (a).
45. Reads/writes requests to I/O devices, are called
a. Input request
b. Output request
c. I/O requests
d. Peripheral requests
Answer: (c).
46. The average time for reading/writing the 512-byte sector for the disk rotating at 10,000 RPM when its time is 6 ms, its transfer rate is 50 MB/sec, and its controller overhead is 0.2 ms
a. 2ms
b. 3.3ms
c. 4.7ms
d. 5ms
Answer: (c).
47. 1GB of data is referred in bytes as

a. 1,000,000,000 bytes
b. 1,000,000,0 bytes
c. 1,000,000 bytes
d. 1,00,000,000 bytes
Answer: (a).
48. A bus which is designed for allowing processors, I/O devices and memory, is called a
a. Processor-memory bus
b. Bus transaction
c. Synchronous bus
d. Backplane bus
Answer: (d).
49. When the disks rotate at 5400 RPM-15,000 RPM, then they have average rotational latency is between
a. 1ms
b. 1.2ms
c. 1.5ms
d. 2.0 ms
Answer: (d).
50. The 32-bit, 33MHz PCI bus will have peak bandwidth of about
a. 111 MB/sec
b. 123 MB/sec
c. 143 MB/sec
d. 133 MB/sec
Answer: (d).
51. Spread of data in the multiple disks, is refered to as
a. SCSI
b. RAID
c. Striping
d. Hit rate
Answer: (c).
52. The data transfer rate is given by the formula
a. Transfer size- transfer time
b. Transfer size transfer time
c. Transfer size+transfer time
d. Transfer size*transfer time
Answer: (b).
53. Measuring the continuous service accomplishment and equivalently of the time to failure from a reference point is called
a. Reference
b. Reliability
c. Hit time
d. Hit rate
Answer: (b).
54. The higher availability cost is reduced to 1/N, where N is the

a. No of disks
b. Reliability
c. Seek
d. Bit rate
Answer: (a).
55. A scheme in which portions of the I/O address space are given to I/O devices, is called
a. Data mapped
b. Memory-mapped I/O
c. Backplane
d. both a and b
Answer: (b).
56. To improve the availability of storage of disk, leveraging redundancy is captured in the
a. SCSI
b. RAID
c. SRAM
d. DRAM
Answer: (b).
57. The hardware component replacing while the system is being run, is known as
a. Cold swapping
b. Blocking cache
c. Hit time
d. Hot swapping
Answer: (d).
58. For accessing data, the operating system must direct the disk using three-stage process called
a. Seek
b. Peek
c. Geek
d. Leek
Answer: (a).
59. The peak rate which transfer data between the I/O device and the main-memory, is known as
a. Bit rate
b. Data rate
c. Hit time
d. Hit miss
Answer: (b).