COMPUTER ORGANIZATION

Functional units of computer

1. The __ format is usually used to store data.

a) BCD b) Decimal c) Hexadecimal d) Octa

2. The 8-bit encoding format used to store data in a computer is __

a) ASCII b) EBCDIC c) ANCI d) USCII

3. A source program is usually in ___

a) Assembly language b) Machine level language c) High-level language d) Natural language

4. Which memory device is generally made of semiconductors?

a) RAM b) Hard-disk c) Floppy disk d) Cd disk

5. The small extremely fast, RAM's are called as ___

a) Cache b) Heaps c) Accumulators d) Stacks

6. The ALU makes use of ___ to store the intermediate results.

a) Accumulators b) Registers c) Heap d) Stack

7. The control unit controls other units by generating _____

a) Control signals b) Timing signals c) Transfer signals d) Command Signals

8. __ are numbers and encoded characters, generally used as operands.

a) Input b) Data c) Information d) Stored Values

9. The Input devices can send information to the processor.

a) When the SIN status flag is set b) When the data arrives regardless of the SIN flag

c) Neither of the cases d) Either of the cases

10. __ bus structure is usually used to connect I/O devices.

a) Single bus b) Multiple bus c) Star bus d) Rambus

11. The I/O interface required to connect the I/O device to the bus consists of __

a) Address decoder and registers b) Control circuits

c) Address decoder, registers and Control circuits d) Only Control circuits

12. To reduce the memory access time we generally make use of __

a) Heaps b) Higher capacity RAM's c) SDRAM's d) Cache's

13. __ is generally used to increase the apparent size of physical memory.

a) Secondary memory b) Virtual memory c) Hard-disk d) Disks

14. MFC stands for _____

a) Memory Format Caches b) Memory Function Complete

c) Memory Find Command d) Mass Format Command

15. The time delay between two successive initiations of memory operation ___

a) Memory access time b) Memory search time

c) Memory cycle time d) Instruction delay

ANSWER:

1.A 2.B 3.C 4.A 5.A 6. A 7. B 8. B 9. A 10. A 11. D 12. B 13. B 14. B 15. C

Basic Operational Concept

1. The decoded instruction is stored in _____
a) IR b) PC c) Registers d) MDR
2. The instruction -> Add LOCA, R0 does _____
a) Adds the value of LOCA to R0 and stores in the temp register
b) Adds the value of R0 to the address of LOCA
c) Adds the values of both LOCA and R0 and stores it in R0
d) Adds the value of LOCA with a value in accumulator and stores it in R0
3. Which registers can interact with the secondary storage?
a) MAR b) PC c) IR d) R0
4. During the execution of a program which gets initialized first?
a) MDR b) IR c) PC d) MAR
5. Which of the register/s of the processor is/are connected to Memory Bus?
a) PC b) MAR c) IR d) Both PC and MAR
6. ISP stands for _____
a) Instruction Set Processor b) Information Standard Processing
c) Interchange Standard Protocol d) Interrupt Service Procedure
7. The internal components of the processor are connected by _____
a) Processor intra-connectivity circuitry b) Processor bus
c) Memory bus d) Rambus

8. _____ is used to choose between incrementing the PC or performing ALU operations.
a) Conditional codes b) Multiplexer c) Control unit d) None of the mentioned
9. The registers, ALU and the interconnection between them are collectively called as _____
a) process route b) information trail c) information path d) data path
10. _____ is used to store data in registers.
a) D flip flop b) JK flip flop c) RS flip flop d) None of the mentioned

ANSWERS:
1.A 2.C 3.A 4.C 5.B 6.A 7.B 8.B 8.D 10.A

Bus stracture

1. The main virtue for using single Bus structure is ____

a) Fast data transfers b) Cost effective connectivity and speed

c) Cost effective connectivity and ease of attaching peripheral devices d) None of the mentioned

2. __ are used to overcome the difference in data transfer speeds of various devices.

a) Speed enhancing circuitory b) Bridge circuits c) Multiple Buses d) Buffer registers

3. To extend the connectivity of the processor bus we use ____

a) PCI bus b) SCSI bus c) Controllers d) Multiple bus

4. IBM developed a bus standard for their line of computers 'PC AT' called ___

a) IB bus b) M-bus c) ISA d) None of the mentioned

5. The bus used to connect the monitor to the CPU is __

a) PCI bus b) SCSI bus c) Memory bus d) Rambus

6. ANSI stands for ____

a) American National Standards Institute b) American National Standard Interface

c) American Network Standard Interfacing d) American Network Security Interrupt

7. ___ register Connected to the Processor bus is a single-way transfer capable.

a) PC b) IR c) Temp d) Z

8. In multiple Bus organisation, the registers are collectively placed and referred as __

a) Set registers b) Register file c) Register Block d) Map registers

9. The main advantage of multiple bus organisation over a single bus is ___

a) Reduction in the number of cycles for execution b) Increase in size of the registers

c) Better Connectivity d) None of the mentioned

10. The ISA standard Buses are used to connect _____

a) RAM and processor b) GPU and processor c) Harddisk and Processor d) CD/DVD drives and Processor

ANSWERS:

1.C 2.D 3.A 4.C 5.B 6.A 7.D 8.B 9.A 10.C

Performance of a System

1. During the execution of the instructions, a copy of the instructions is placed in the _____

a) Register b) RAM c) System heap d) Cache

2. Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster?
a) A b) B c) Both take the same time d) Insufficient information

3. A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____
a) Super-scaling b) Pipe-lining c) Parallel Computation d) None of the mentioned

4. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution?
a) ISA b) ANSA c) Super-scalar d) All of the mentioned

5. The clock rate of the processor can be improved by _____
a) Improving the IC technology of the logic circuits b) Reducing the amount of processing done in one step

c) By using the overclocking method d) All of the mentioned

6. An optimizing Compiler does _____
a) Better compilation of the given piece of code and reduces its process time b) Takes advantage of the type of processor
c) Does better memory management d) None of the mentioned

7. The ultimate goal of a compiler is to _____
a) Reduce the clock cycles for a programming task b) Reduce the size of the object code
c) Be versatile d) Be able to detect even the smallest of errors

8. SPEC stands for _____
a) Standard Performance Evaluation Code b) System Processing Enhancing Code
c) System Performance Evaluation Corporation d) Standard Processing Enhancement Corporation

9. As of 2000, the reference system to find the performance of a system is _____
a) Ultra SPARC 10
b) SUN SPARC
c) SUN II
d) None of the mentioned

10. When Performing a looping operation, the instruction gets stored in the _____
a) Registers b) Cache c) System Heap d) System stack

11. The average number of steps taken to execute the set of instructions can be made to be less than one by following _____
a) ISA b) Pipe-lining c) Super-scaling d) Sequential

12. If a processor clock is rated as 1250 million cycles per second, then its clock period is _____
a) $1.9 * 10^{-10}$ sec b) $1.6 * 10^{-9}$ sec c) $1.25 * 10^{-10}$ sec d) $8 * 10^{-10}$ sec

13. If the instruction, Add R1, R2, R3 is executed in a system that is pipe-lined, then the value of S is (Where S is a term of the Basic performance equation)?
a) 3 b) ~2 c) ~1 d) 6

14. CISC stands for _____
a) Complete Instruction Sequential Compilation b) Computer Integrated Sequential Compiler
c) Complex Instruction Set Computer d) Complex Instruction Sequential Compilation

Ans: C

15. As of 2000, the reference system to find the SPEC rating are built with _____ Processor.
a) Intel Atom SParc 300Mhz b) Ultra SPARC -IIi 300MHZ
c) Amd Neutrino series d) ASUS A series 450 Mhz

ANSWERS:

1.D 2.A 3.B 4.C 5.D 6.B 7.A 8.C 9.A 10.B 11.C 12.D 13.C 14.C 15.B

Addressing Modes

1. The instruction, Add #45,R1 does _____
   a) Adds the value of 45 to the address of R1 and stores 45 in that address

b) Adds 45 to the value of R1 and stores it in R1

c) Finds the memory location 45 and adds that content to that of R1

d) None of the mentioned

2. In the case of, Zero-address instruction method the operands are stored in _____

a) Registers b) Accumulators c) Push down stack d) Cache

3. Add #45, when this instruction is executed the following happen/s _____

a) The processor raises an error and requests for one more operand

b) The value stored in memory location 45 is retrieved and one more operand is requested

c) The value 45 gets added to the value on the stack and is pushed onto the stack

d) None of the mentioned

4. The addressing mode which makes use of in-direction pointers is _____

a) Indirect addressing mode b) Index addressing mode

c) Relative addressing mode d) Offset addressing mode

5. In the following indexed addressing mode instruction, MOV 5(R1), LOC the effective address is _____

a) EA = 5+R1 b) EA = R1 c) EA = [R1] d) EA = 5+[R1]

6. The addressing mode/s, which uses the PC instead of a general purpose register is _____

a) Indexed with offset b) Relative c) Direct d) Both Indexed with offset and direct

7. When we use auto increment or auto decrements, which of the following is/are true?

1) In both, the address is used to retrieve the operand and then the address gets altered

2) In auto increment, the operand is retrieved first and then the address altered

3) Both of them can be used on general purpose registers as well as memory locations

a) 1, 2, 3 b) 2 c) 1, 3 d) 2, 3

8. The addressing mode, where you directly specify the operand value is _____

a) Immediate b) Direct c) Definite d) Relative

9. The effective address of the following instruction is MUL 5(R1,R2).

a) 5+R1+R2 b) 5+(R1*R2) c) 5+[R1]+[R2] d) 5*([R1]+[R2])

10. _____ addressing mode is most suitable to change the normal sequence of execution of instructions.

a) Relative b) Indirect c) Index with Offset d) Immediate

ANSWERS:

1.B 2.C 3.B 4.A 5.D 6.B 7.D 8.A 9.C 10.A

Numbers and Arithmetic Operations

1. Which method/s of representation of numbers occupies a large amount of memory than others?

a) Sign-magnitude b) 1's complement c) 2's complement d) 1's & 2's compliment

2. Which representation is most efficient to perform arithmetic operations on the numbers?
a) Sign-magnitude b) 1's complement c) 2'S complement d) None of the mentioned

3. Which method of representation has two representations for '0'?
a) Sign-magnitude b) 1's complement c) 2's complement d) None of the mentioned

4. When we perform subtraction on -7 and 1 the answer in 2's complement form is _____
a) 1010 b) 1110 c) 0110 d) 1000

5. When we perform subtraction on -7 and -5 the answer in 2's complement form is _____
a) 11110 b) 1110 c) 1010 d) 0010

6. When we subtract -3 from 2 , the answer in 2's complement form is _____
a) 0001 b) 1101 c) 0101 d) 1001

7. The processor keeps track of the results of its operations using flags called _____
a) Conditional code flags b) Test output flags c) Type flags d) None of the mentioned

8. The register used to store the flags is called as _____
a) Flag register b) Status register c) Test register d) Log register

9. The Flag 'V' is set to 1 indicates that _____
a) The operation is valid b) The operation is validated
c) The operation has resulted in an overflow d) None of the mentioned

10. In some pipelined systems, a different instruction is used to add to numbers which can affect the flags upon execution. That instruction is _____
a) AddSetCC b) AddCC c) Add++ d) SumSetCC

11. The most efficient method followed by computers to multiply two unsigned numbers is _____
a) Booth algorithm b) Bit pair recording of multipliers
c) Restoring algorithm d) Non restoring algorithm

12. For the addition of large integers, most of the systems make use of _____
a) Fast adders b) Full adders c) Carry look-ahead adders d) None of the mentioned

13. In a normal n-bit adder, to find out if an overflow as occurred we make use of _____
a) And gate b) Nand gate c) Nor gate d) Xor gate

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a) And gate b) Nand gate c) Nor gate d) Xor gate
14. In the implementation of a Multiplier circuit in the system we make use of _____
a) Counter b) Flip flop c) Shift register d) Push down stack
15. When 1101 is used to divide 100010010 the remainder is _____
a) 101 b) 11 c) 0 d) 1

ANSWERS:
1.A 2.C 3.A 4.D 5.B 6.C 7.A 8.B 9.C 10.A 11.B 12.C 13.D 14.C 15.D

Instructions and Instruction Sequencing

1. RTN stands for _____
a) Register Transfer Notation b) Register Transmission Notation
c) Regular Transmission Notation d) Regular Transfer Notation
2. The instruction, Add Loc,R1 in RTN is _____
a) AddSetCC Loc+R1 b) R1=Loc+R1
c) Not possible to write in RTN d) R1<-[Loc]+[R1]
3. Can you perform an addition on three operands simultaneously in ALN using Add instruction?
a) Yes b) Not possible using Add, we've to use AddSetCC
c) Not permitted d) None of the mentioned
4. The instruction, Add R1,R2,R3 in RTN is _____
a) R3=R1+R2+R3 b) R3<-[R1]+[R2]+[R3] c) R3=[R1]+[R2] d) R3<-[R1]+[R2]
5. In a system, which has 32 registers the register id is _____ long.
a) 16 bit b) 8 bits c) 5 bits d) 6 bits
6. The two phases of executing an instruction are _____
a) Instruction decoding and storage b) Instruction fetch and instruction execution
c) Instruction execution and storage d) Instruction fetch and Instruction processing
7. The Instruction fetch phase ends with _____
a) Placing the data from the address in MAR into MDR
b) Placing the address of the data into MAR
c) Completing the execution of the data and placing its storage address into MAR
d) Decoding the data in MDR and placing it in IR
8. While using the iterative construct (Branching) in execution _____

instruction is used to check the condition.
a) TestAndSet b) Branch c) TestCondn d) None of the mentioned
9. When using Branching, the usual sequencing of the PC is altered. A new instruction is loaded which is called as _____
a) Branch target b) Loop target c) Forward target d) Jump instruction
10. The condition flag Z is set to 1 to indicate _____
a) The operation has resulted in an error b) The operation requires an interrupt call
c) The result is zero d) There is no empty register available

ANSWER:

1.A 2.D 3.C 4.D 5.C 6.B 7.D 8.B 9.A 10.C

Accessing I/O Devices:

1. In memory-mapped I/O _____
a) The I/O devices and the memory share the same address space
b) The I/O devices have a separate address space
c) The memory and I/O devices have an associated address space
d) A part of the memory is specifically set aside for the I/O operation

2. The usual BUS structure used to connect the I/O devices is _____
a) Star BUS structure b) Multiple BUS structure
c) Single BUS structure d) Node to Node BUS structure

3. In intel's IA-32 architecture there is a separate 16 bit address space for the I/O devices.
a) False b) True

4. The advantage of I/O mapped devices to memory mapped is _____
a) The former offers faster transfer of data
b) The devices connected using I/O mapping have a bigger buffer space
c) The devices have to deal with fewer address lines
d) No advantage as such

5. The system is notified of a read or write operation by _____
a) Appending an extra bit of the address b) Enabling the read or write bits of the devices
c) Raising an appropriate interrupt signal d) Sending a special signal along the BUS

6. To overcome the lag in the operating speeds of the I/O device and the processor we use _____
a) BUffer spaces b) Status flags c) Interrupt signals d) Exceptions
7. The method of accessing the I/O devices by repeatedly checking the status flags is _____
a) Program-controlled I/O b) Memory-mapped I/O c) I/O mapped d) None of the mentioned

8. The method of synchronising the processor with the I/O device in which the device sends a signal when it is ready is?
a) Exceptions b) Signal handling c) Interrupts d) DMA
9. The method which offers higher speeds of I/O transfers is _____
a) Interrupts b) Memory mapping c) Program-controlled I/O d) DMA

10. The process wherein the processor constantly checks the status flags is called as _____
a) Polling b) Inspection c) Reviewing d) Echoing

ANSWERS:

1.A 2.C 3.B 4.C 5.D 6.B 7.A 8.C 9.D 10.A

Interrupts – 1:

1. The interrupt-request line is a part of the _____
a) Data line b) Control line c) Address line d) None of the mentioned
2. The return address from the interrupt-service routine is stored on the _____
a) System heap b) Processor register c) Processor stack d) Memory
3. The signal sent to the device from the processor to the device after receiving an interrupt is _____
a) Interrupt-acknowledge b) Return signal c) Service signal d) Permission signal
4. When the process is returned after an interrupt service _____ should be loaded again.
i) Register contents
ii) Condition codes
iii) Stack contents
iv) Return addresses
a) i, iv b) ii, iii and iv c) iii, iv d) i, ii
5. The time between the receiver of an interrupt and its service is _____
a) Interrupt delay b) Interrupt latency c) Cycle time d) Switching time
6. Interrupts form an important part of _____ systems.
a) Batch processing b) Multitasking c) Real-time processing d) Multi-user
7. A single Interrupt line can be used to service n different devices.
a) True b) False
8. _____ type circuits are generally used for interrupt service lines.
i) open-collector
ii) open-drain
iii) XOR
iv) XNOR
a) i, ii b) ii c) ii, iii d) ii, iv

9. The resistor which is attached to the service line is called _____
a) Push-down resistor b) Pull-up resistor
c) Break down resistor d) Line resistor
10. An interrupt that can be temporarily ignored is _____
a) Vectored interrupt b) Non-maskable interrupt
c) Maskable interrupt d) High priority interrupt
11. The 8085 microprocessor responds to the presence of an interrupt _____
a) As soon as the trap pin becomes 'LOW'
b) By checking the trap pin for 'high' status at the end of each instruction fetch
c) By checking the trap pin for 'high' status at the end of execution of each instruction
d) By checking the trap pin for 'high' status at regular intervals
12. CPU as two modes privileged and non-privileged. In order to change the mode from privileged to non-privileged.
a) A hardware interrupt is needed b) A software interrupt is needed
c) Either hardware or software interrupt is needed
d) A non-privileged instruction (which does not generate an interrupt)is needed
13. Which interrupt is unmaskable?
a) RST 5.5 b) RST 7.5 c) TRAP d) Both RST 5.5 and 7.5
14. From amongst the following given scenarios determine the right one to justify interrupt mode of data transfer.
i) Bulk transfer of several kilo-byte ii) Moderately large data transfer of more than 1kb
iii) Short events like mouse action iv) Keyboard inputs
a) i and ii b) ii c) i, ii and iv d) iv
15. How can the processor ignore other interrupts when it is servicing one _____
a) By turning off the interrupt request line
b) By disabling the devices from sending the interrupts
c) BY using edge-triggered request lines
d) All of the mentioned

NASWERS:

1.B 2.C 3.A 4.D 5.B 6.C 7.A 8.A 9.B 10.C 11.C 12.B 13.C 14.D 15.D

Interrupts – 2:

1. When dealing with multiple devices interrupts, which mechanism is easy to implement?
a) Polling method b) Vectored interrupts c) Interrupt nesting d) None of the mentioned
2. The interrupt servicing mechanism in which the requesting device identifies itself to the processor to be serviced is _____
a) Polling `b) Vectored interrupts c) Interrupt nesting d) Simultaneous requesting
3. In vectored interrupts, how does the device identify itself to the processor?
a) By sending its device id b) By sending the machine code for the interrupt service

routine
c) By sending the starting address of the service routine d) None of the mentioned
4. The code sent by the device in vectored interrupt is _____ long.
a) upto 16 bits b) upto 32 bits c) upto 24 bits d) 4-8 bits
5. The starting address sent by the device in vectored interrupt is called as _____
a) Location id b) Interrupt vector c) Service location d) Service id
6. The processor indicates to the devices that it is ready to receive interrupts _____
a) By enabling the interrupt request line b) By enabling the IRQ bits
c) By activating the interrupt acknowledge line d) None of the mentioned
7. We describe a protocol of input device communication below:
i) Each device has a distinct address.
ii) The BUS controller scans each device in a sequence of increasing address value to determine if the entity wishes to communicate
iii) The device ready to communicate leaves its data in the I/O register
iv) The data is picked up and the controller moves to the step a
Identify the form of communication best describes the I/O mode amongst the following.
a) Programmed mode of data transfer b) DMA c) Interrupt mode d) Polling
8. Which one of the following is true with regard to a CPU having a single interrupt request line and single interrupt grant line?
i) Neither vectored nor multiple interrupting devices is possible.
ii) Vectored interrupts is not possible but multiple interrupting devices is possible.
iii) Vectored interrupts is possible and multiple interrupting devices is not possible.
iv) Both vectored and multiple interrupting devices are possible.
a) iii b) i, iv c) ii, iii d) iii, iv
9. Which table handle stores the addresses of the interrupt handling sub-routines?
a) Interrupt-vector table b) Vector table c) Symbol link table d) None of the mentioned
10. _____ method is used to establish priority by serially connecting all devices that request an interrupt.
a) Vectored-interrupting b) Daisy chain c) Priority d) Polling
11. In daisy chaining device 0 will pass the signal only if it has _____
a) Interrupt request b) No interrupt request
c) Both No interrupt and Interrupt request d) None of the mentioned
12. _____ interrupt method uses register whose bits are set separately by interrupt signal for each device.
a) Parallel priority interrupt b) Serial priority interrupt
c) Daisy chaining d) None of the mentioned
13. _____ register is used for the purpose of controlling the status of each interrupt request in parallel priority interrupt.
a) Mass b) Mark c) Make d) Mask
14. The added output of the bits of the interrupt register and the mask register is set as an input of _____
a) Priority decoder b) Priority encoder c) Process id encoder d) Multiplexer
15. Interrupts initiated by an instruction is called as _____
a) Internal b) External c) Hardware d) Software

ANSWERS:

1.A 2.B 3.C 4.D 5.B 6.C 7.D 8.A 9.A 10.B 11.B 12.A 13.D 14.B 15.B

Direct Memory Access:

1. The DMA differs from the interrupt mode by _____
a) The involvement of the processor for the operation
b) The method of accessing the I/O devices
c) The amount of data transfer possible
d) None of the mentioned
2. The DMA transfers are performed by a control circuit called as _____
a) Device interface b) DMA controller c) Data controller d) Overlooker
3. In DMA transfers, the required signals and addresses are given by the _____
a) Processor b) Device drivers c) DMA controllers d) The program itself
4. After the completion of the DMA transfer, the processor is notified by _____
a) Acknowledge signal b) Interrupt signal c) WMFC signald) None of the mentioned
5. The DMA controller has _____ registers.
a) 4 b) 2 c) 3 d) 1
6. When the R/W bit of the status register of the DMA controller is set to 1.
a) Read operation is performed b) Write operation is performed
c) Read & Write operation is performed d) None of the mentioned
7. The controller is connected to the ____
a) Processor BUS b) System BUS c) External BUS d) None of the mentioned
8. Can a single DMA controller perform operations on two different disks simultaneously?
a) True b) False
9. The technique whereby the DMA controller steals the access cycles of the processor to operate is called _____
a) Fast conning b) Memory Con c) Cycle stealing d) Memory stealing
10. The technique where the controller is given complete access to main memory is _____
a) Cycle stealing b) Memory stealing c) Memory Con d) Burst mode
11. The controller uses _____ to help with the transfers when handling network interfaces.
a) Input Buffer storage b) Signal enhancers c) Bridge circuits d) All of the mentioned
12. To overcome the conflict over the possession of the BUS we use _____
a) Optimizersb) BUS arbitrators c) Multiple BUS structure d) None of the mentioned
13. The registers of the controller are _____
a) 64 bits b) 24 bits c) 32 bits d) 16 bits
14. When the process requests for a DMA transfer?
a) Then the process is temporarily suspended b) The process continues execution
c) Another process gets executed d) process is temporarily suspended & Another process gets executed
15. The DMA transfer is initiated by _____
a) Processor b) The process being executed c) I/O devices d) OS

ANSWERS:

1.D 2.B 3.C 4.B 5.C 6.A 7.B 8.A 9.C 10.D 11.A 12.B 13.C 14.D 15.C

Hierarchy of Memory:

1. The standard SRAM chips are costly as _____
a) They use highly advanced micro-electronic devices
b) They house 6 transistor per chip
c) They require specially designed PCB's
d) None of the mentioned
2. The drawback of building a large memory with DRAM is _____
a) The large cost factor b) The inefficient memory organisation
c) The Slow speed of operation d) All of the mentioned
3. To overcome the slow operating speeds of the secondary memory we make use of faster flash drives.
a) True b) False
4. The fastest data access is provided using _____
a) Caches b) DRAM's c) SRAM's d) Registers

5. The memory which is used to store the copy of data or instructions stored in larger memories, inside the CPU is called _____
a) Level 1 cache b) Level 2 cache c) Registers d) TLB
View Answer
6. The larger memory placed between the primary cache and the memory is called _____
a) Level 1 cache b) Level 2 cache c) EEPROM d) TLB
7. The next level of memory hierarchy after the L2 cache is _____
a) Secondary storage b) TLB c) Main memory d) Register
8. The last on the hierarchy scale of memory devices is _____
a) Main memory b) Secondary memory c) TLBd) Flash drives
9. In the memory hierarchy, as the speed of operation increases the memory size also increases.
a) True b) False
10. If we use the flash drives instead of the harddisks, then the secondary storage can go above primary memory in the hierarchy.
a) True b) False

ANSWERS:

1.B 2.C 3.A 4.D 5.A 6.B 7.D 8.B 9.B 10.B

Caches:

1. The reason for the implementation of the cache memory is _____
a) To increase the internal memory of the system
b) The difference in speeds of operation of the processor and memory
c) To reduce the memory access and cycle time

d) All of the mentioned
2. The effectiveness of the cache memory is based on the property of _____
a) Locality of reference b) Memory localisation
c) Memory size d) None of the mentioned
3. The temporal aspect of the locality of reference means _____
a) That the recently executed instruction won't be executed soon
b) That the recently executed instruction is temporarily not referenced
c) That the recently executed instruction will be executed soon again
d) None of the mentioned
4. The spatial aspect of the locality of reference means _____
a) That the recently executed instruction is executed again next
b) That the recently executed won't be executed again
c) That the instruction executed will be executed at a later time
d) That the instruction in close proximity of the instruction executed will be executed in future
5. The correspondence between the main memory blocks and those in the cache is given by _____
a) Hash function b) Mapping function c) Locale function d) Assign function
6. The algorithm to remove and place new contents into the cache is called _____
a) Replacement algorithm b) Renewal algorithm c) Updation d) None of the mentioned
7. The write-through procedure is used _____
a) To write onto the memory directly
b) To write and read from memory simultaneously
c) To write directly on the memory and the cache simultaneously
d) None of the mentioned
8. The bit used to signify that the cache location is updated is _____
a) Dirty bit b) Update bit c) Reference bit d) Flag bit
9. The copy-back protocol is used _____
a) To copy the contents of the memory onto the cache
b) To update the contents of the memory from the cache
c) To remove the contents of the cache and push it on to the memory
d) None of the mentioned
10. The approach where the memory contents are transferred directly to the processor from the memory is called _____
a) Read-later b) Read-through c) Early-start d) None of the mentioned

ANSWERS:

1.B 2.A 3.C 4.D 5.B 6.A 7.C 8.A 9.B 10.C

Mapping Functions:

1. The memory blocks are mapped on to the cache with the help of _____
a) Hash functions b) Vectors c) Mapping functions d) None of the mentioned

2. During a write operation if the required block is not present in the cache then _____ occurs.
a) Write latency b) Write hit c) Write delay d) Write miss
3. In _____ protocol the information is directly written into the main memory.
a) Write through b) Write back c) Write first d) None of the mentioned
4. The only draw back of using the early start protocol is _____
a) Time delay b) Complexity of circuit c) Latency d) High miss rate
5. The method of mapping the consecutive memory blocks to consecutive cache blocks is called _____
a) Set associative b) Associative c) Direct d) Indirect
6. While using the direct mapping technique, in a 16 bit system the higher order 5 bits are used for _____
a) Tag b) Block c) Word d) Id
7. In direct mapping the presence of the block in memory is checked with the help of block field.
a) True b) False
8. In associative mapping, in a 16 bit system the tag field has _____ bits.
a) 12 b) 8 c) 9 d) 10
9. The associative mapping is costlier than direct mapping.
a) True b) False
10. The technique of searching for a block by going through all the tags is _____
a) Linear search b) Binary search c) Associative search d) None of the mentioned
11. The set-associative map technique is a combination of the direct and associative technique.
a) True b) False
12. In set-associative technique, the blocks are grouped into _____ sets.
a) 4 b) 8 c) 12 d) 6
13. A control bit called _____ has to be provided to each block in set-associative.
a) Idol bit b) Valid bit c) Reference bit d) All of the mentioned
14. The bit used to indicate whether the block was recently used or not is _____
a) Idol bit b) Control bit c) Reference bit d) Dirty bit
15. Data which is not up-to date is called as _____
a) Spoilt data b) Stale data c) Dirty data d) None of the mentioned

ANSWERS:

1.C 2.D 3.A 4.B 5.C 6.A 7.B 8.A 9.A 10.C 11.A 12.D 13.B 14.D 15.B

Performance of Caches:

1. The key factor/s in commercial success of a computer is/are _____
a) Performance b) Cost c) Speed d) Both Performance and Cost
2. The main objective of the computer system is _____
a) To provide optimal power operation b) To provide the best performance at low cost
c) To provide speedy operation at low power consumption d) All of the mentioned

3. A common measure of performance is _____
a) Price/performance ratio b) Performance/price ratio
c) Operation/price ratio d) None of the mentioned
4. The performance depends on _____
a) The speed of execution only b) The speed of fetch and execution
c) The speed of fetch only d) The hardware of the system only
5. The main purpose of having memory hierarchy is to _____
a) Reduce access time b) Provide large capacity
c) Reduce propagation time d) Reduce access time & Provide large capacity
6. The memory transfers between two variable speed devices are always done at the speed of the faster device.
a) True b) False
7. An effective to introduce parallelism in memory access is by _____
a) Memory interleaving b) TLB c) Pages d) Frames
8. The performance of the system is greatly influenced by increasing the level 1 cache.
a) True b) False
9. Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster.
a) A b) B c) Both take the same time d) Insufficient information
10. If the instruction Add R1, R2, R3 is executed in a system which is pipelined, then the value of S is (Where S is a term of the Basic performance equation).
a) 3 b) ~2 c) ~1 d) 6

ANSWERS:

1.D 2.B 3.A 4.B 5.D 6.A 7.A 8.A 9.A 10.C

Virtual Memory:

1. The physical memory is not as large as the address space spanned by the processor.
a) True b) False
2. The program is divided into operable parts called as _____
a) Frames b) Segments c) Pages d) Sheets
3. The techniques which move the program blocks to or from the physical memory is called as _____
a) Paging b) Virtual memory organization c) Overlays d) Framing
4. The binary address issued to data or instructions are called as _____
a) Physical address b) Location c) Relocatable address d) Logical address
5. _____ is used to implement virtual memory organisation.
a) Page table b) Frame table c) MMU d) None of the mentioned
6. _____ translates the logical address into a physical address.
a) MMU b) Translator c) Compiler d) Linker

7. The main aim of virtual memory organisation is _____
a) To provide effective memory access b) To provide better memory transfer
c) To improve the execution of the program d) All of the mentioned
8. The DMA doesn't make use of the MMU for bulk data transfers.
a) True b) False
9. The virtual memory basically stores the next segment of data to be executed on the _____
a) Secondary storage b) Disks c) RAM d) ROM
10. The associatively mapped virtual memory makes use of _____
a) TLB b) Page tablec) Frame table d) None of the mentioned

ANSWERS:

1.A 2.B 3.B 4.D 5.C 6.A 7.D 8.B 9.A 10.A

Representation of Floating Number:

1. The decimal numbers represented in the computer are called as floating point numbers, as the decimal point floats through the number.
a) True b) False
2. The numbers written to the power of 10 in the representation of decimal numbers are called as _____
a) Height factors b) Size factors c) Scale factors d) None of the mentioned
3. If the decimal point is placed to the right of the first significant digit, then the number is called _____
a) Orthogonal b) Normalized c) Determinate d) None of the mentioned
4. _____ constitute the representation of the floating number.
a) Sign b) Significant digits c) Scale factor d) All of the mentioned
5. The sign followed by the string of digits is called as _____
a) Significant b) Determinant c) Mantissa d) Exponent
6. In IEEE 32-bit representations, the mantissa of the fraction is said to occupy _____ bits.
a) 24 b) 23 c) 20 d) 16
7. The normalized representation of $0.0010110 * 2_9$ is _____
a) 0 10001000 0010110 b) 0 10000101 0110
c) 0 10101010 1110 d) 0 11110100 11100
8. The 32 bit representation of the decimal number is called as _____
a) Double-precision b) Single-precision c) Extended format d) None of the mentioned
9. In 32 bit representation the scale factor as a range of _____
a) -128 to 127 b) -256 to 255 c) 0 to 255 d) None of the mentioned
10. In double precision format, the size of the mantissa is _____
a) 32 bit b) 52 bit c) 64 bit d) 72 bit

ANSWERS:

1.A 2.C 3.B 4.D 5.C 6.B 7.B 8.B 9.A 10.B