EC 23002 Digital Electronics Circuits (3-0-3 5)
Pre- requisite: None

Switching algebra, minimizing functions using maps, different logic families, TTL, ECL, NMOS, CMOS, pass transistor logic, combinational logic circuits:- adders / subtractor, demultiplexers, encoders , decoders , ROMs , PLAs etc. sequential logic circuits:- flip flops and latches , shifters, counters, finite state machine – state transition diagrams and state transition tables. memory elements :- ROM, PROM, RAM-SRAM, DRAM. case studies : a simple computer, RTL – micro-instruction, instruction decoders timing and controller circuits, data path unit.

Sector wise distribution:

1. Switching algebra, minimizing functions using maps
2. Different logic families, TTL, ECL, NMOS, CMOS, pass transistor logic
3. Combinational logic circuits:- adders / subtractor, demultiplexers, encoders , decoders , ROMs , PLAs etc.
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6. Case studies : a simple computer, RTL – micro-instruction, instruction decoders timing and controller circuits, data path unit.

Books: Grinich Jackson, Tocci, Rabaey, Taub, Mano, Yarbrough, Malvino

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Why Digital?

Digital : Processing of discretized information(signal).

1. Accurate.
2. Flexible.
3. It requires less operational energy.
4. Repeatability.
5. ?
6. ?

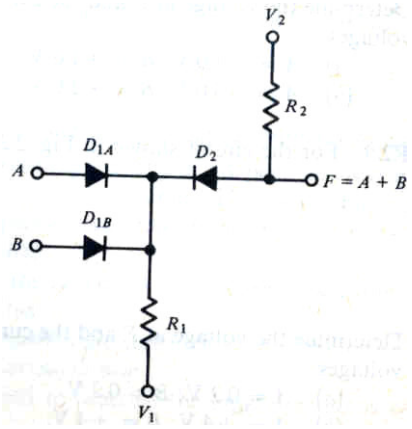
The foundation of any digital system is the logic gate. A variety of electronic circuits exists that can be used as basic logic gates. One logic family is built around one kind of basic circuit.

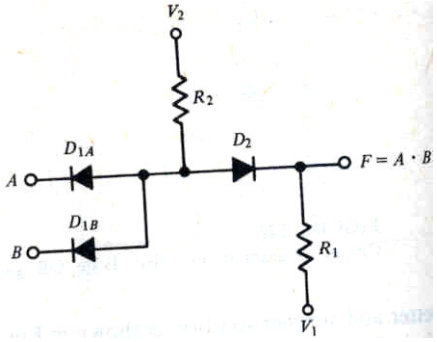
Why Different Logic Families?

1. Space satellite, Digital wristwatch – low power consumption
2. Scientific Computer – high speed
3. Digital Control of equipment in industrial environment – noise immunity
4. Compatibility
5. Flexibility
6. Cost
7. Size, Packing Density
8. Evolution

Transistor-inverter is key to development of logic circuit. Why?

Diodes, Switches can be used to build OR and AND circuit but not NOT circuit. Hence, with these it is not possible to develop every type of logic circuits.





Can you get simpler diode circuits for same logic operations?

A typical transistor inverter

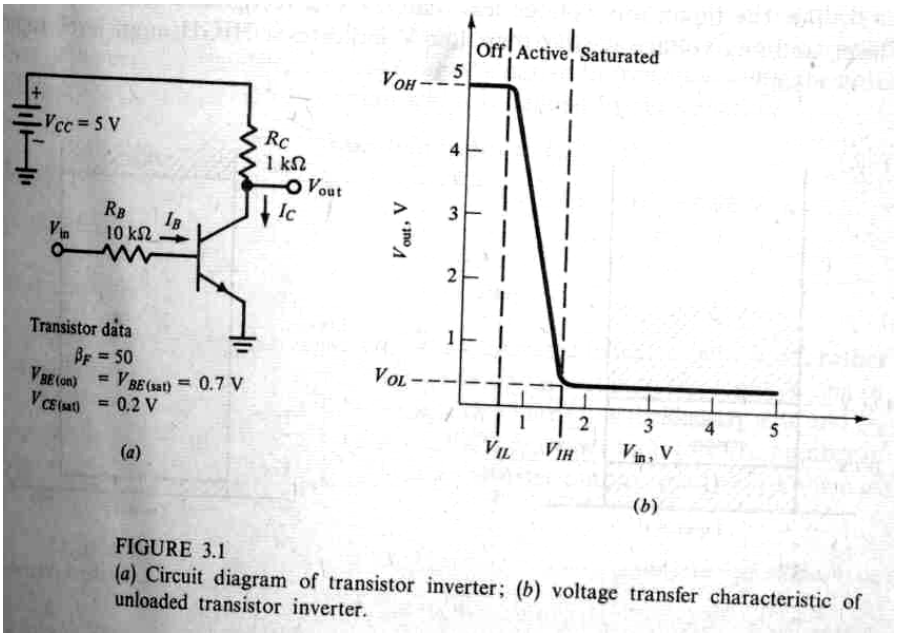


FIGURE 3.1
(*a*) Circuit diagram of transistor inverter; (*b*) voltage transfer characteristic of unloaded transistor inverter.

V_{in} (V)	I_B (mA)	I_C (mA)	V_{out} (V)
0	0	0	5.0
0.5	0	0	5.0
1.0	0.03	1.5	3.5
1.5	0.08	4.0	1.0
2.0	0.13	4.8	0.2
3.0	0.23	4.8	0.2
4.0	0.33	4.8	0.2
5.0	0.43	4.8	0.2

Analysis:

Base current $I_B = 0$ till $V_{BE} < 0.7V$ i.e. $V_{in} < 0.7V$. Transistor is *cut off* and $I_C = 0$ with $V_{out} = 5V$ over entire range.

When V_{in} is increased beyond 0.7V, base current begins to flow and the transistor moves from *cut off* region to *normal active* region. Hence, the coordinates $V_{in} = 0.7V$, $V_{out} = 5V$ mark first transition point in the transfer function of this circuit. This is also termed as *breakpoint* or *edge of cutoff* (EOC).

Now, $I_B = (V_{in} - V_{BE(on)})/R_B$ And $I_C = \beta_F I_B$: as long as $V_{CE} < V_{CE(sat)}$

Then $V_{out} = V_{CC} - \beta_F I_B R_C$ Or, $V_{out} = V_{CC} - \beta_F R_C (V_{in} - V_{BE(on)})/R_B$

Thus V_{out} decreases linearly with increase in V_{in} as long as transistor remains in active mode.

As V_{in} (or I_B) is increased a second transition point is reached when $V_{out} = V_{CE(sat)}$. The values of I_C and I_B for this condition (the subscript EOS means *edge of sturation*):

$I_{C(EOS)} = (V_{CC} - V_{CE(sat)})/R_C = (5\text{-}0.2)/1 = 4.8mA$ and $I_{B(EOS)} = I_{C(EOS)}/\beta_F = 4.8/50 = 0.096mA$

Then $V_{in(EOS)} = V_{BE(on)} + I_{B(EOS)} R_B = 0.7 + (0.096)(10) = 1.66V$

Thus $V_{in} \geq 1.66V$ the transistor saturates. (Saturating Logic)

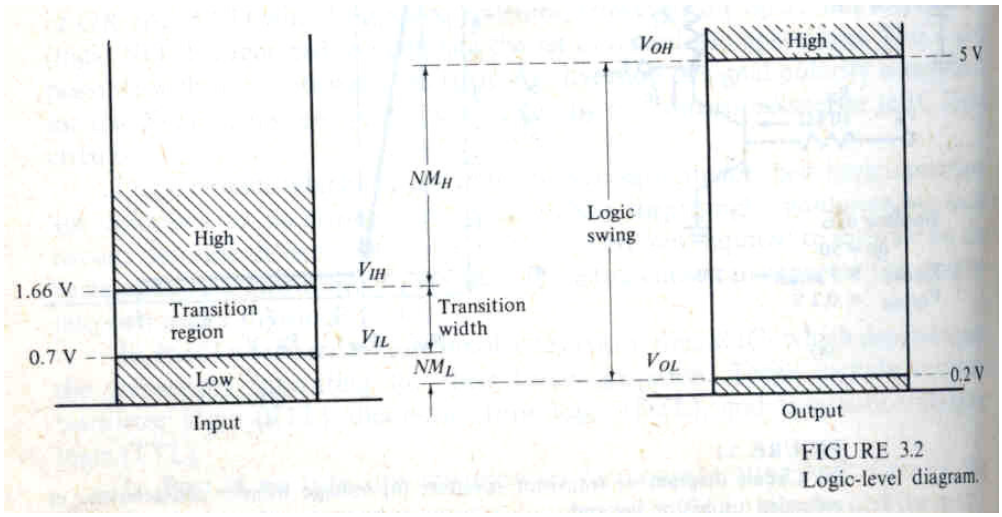


FIGURE 3.2
Logic-level diagram.

V_{IL} = Threshold voltage for LOW level V_{OL} = Threshold voltage for LOW level

V_{IH} = Threshold voltage for HIGH level V_{OH} = Threshold voltage for HIGH level

For the input any voltage $< 0.7V$ is recognized as LOW input level
And any voltage $> 1.66V$ indicates HIGH input level.

At the input side voltage levels between 0.7 to 1.66V are to be avoided because they lead to output voltage levels that are ambiguous.

Logic swing : The difference between the two output voltages = $V_{OH} – V_{OL} = 5 – 0.2 = 4.8V$

Noise Margins

NM_L : LOW level noise margin = $V_{IL} – V_{OL} = 0.7 – 0.2 = 0.5V$

NM_H : HIGH level noise margin = $V_{OH} – V_{IH} = 5.0 – 1.66 = 3.34V$

Noise margin capability increases if V_{OH} and V_{OL} move away from each other i.e. with larger logic swing.

Noise margin capability increases if V_{IH} and V_{IL} move towards each other i.e. with narrower transition width.

Transition width = $V_{IH} - V_{IL} = 1.66 – 0.7 = 0.96V$

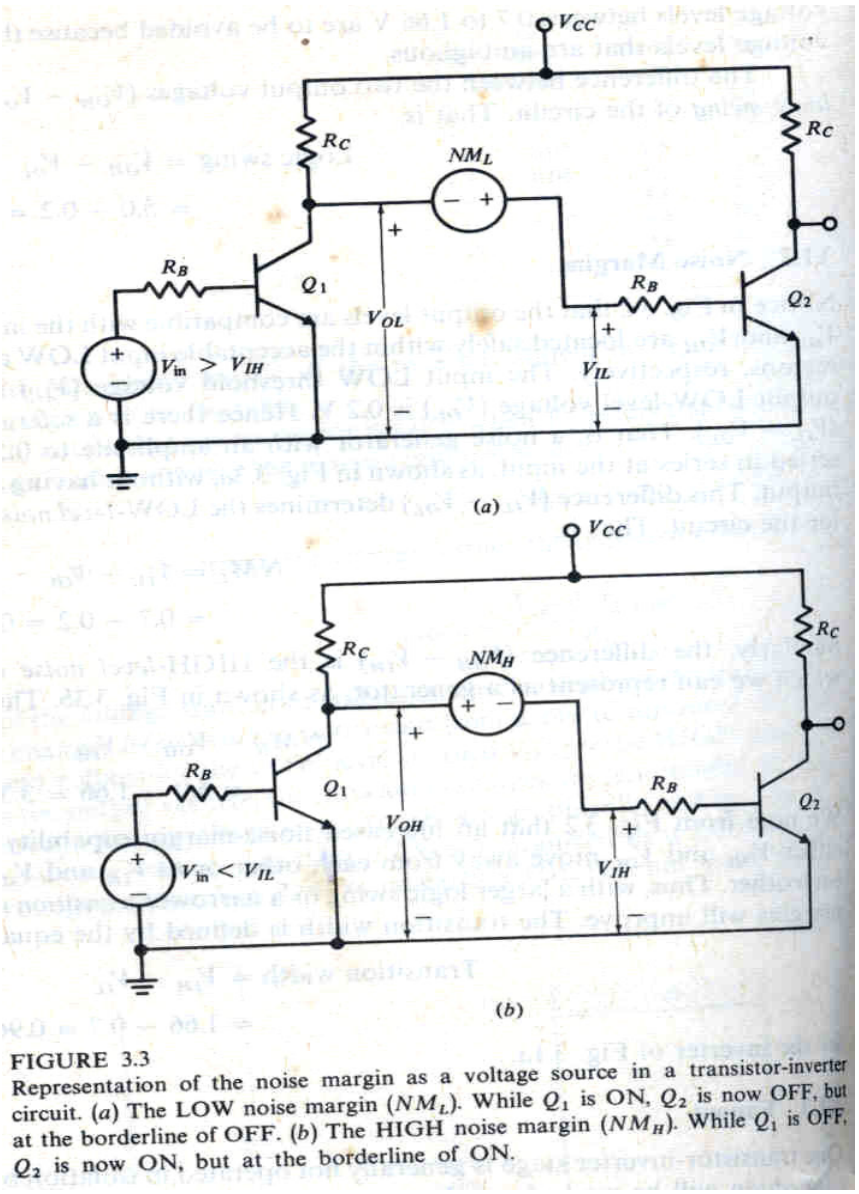


FIGURE 3.3
Representation of the noise margin as a voltage source in a transistor-inverter circuit. (*a*) The LOW noise margin (NM_L). While Q_1 is ON, Q_2 is now OFF, but at the borderline of OFF. (*b*) The HIGH noise margin (NM_H). While Q_1 is OFF, Q_2 is now ON, but at the borderline of ON.

For LOW level input a noise generator of amplitude NM_L (=0.5V) could be inserted in series at the input without having any effect on the output.

Similarly, for HIGH level input a noise generator of amplitude NM_H (=3.34V) could be inserted in series at the input without having any effect on the output.

Note, the polarity of the two noise generator.

Fan out

One logic gate generally is not operated in isolation. Connections are made from output of one to input of one or more similar circuits. The maximum number of such inputs that can be connected is known as *fanout*.

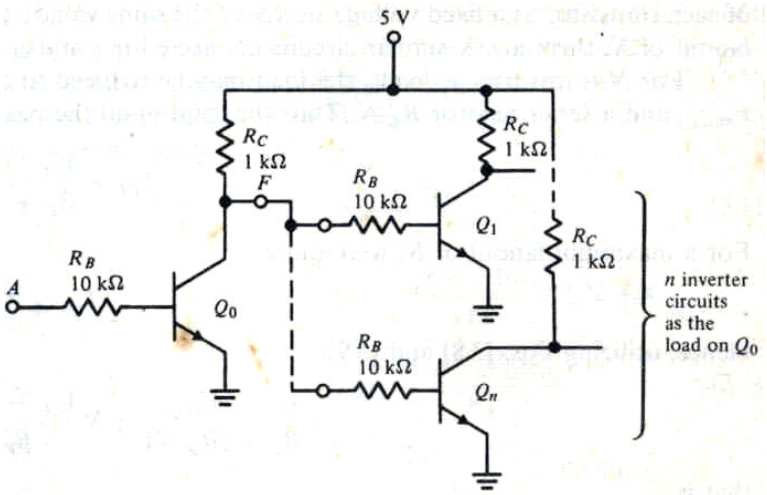


FIGURE 3.4
Transistor-inverter circuit with *n* other inverter inputs as a load.

Fanout Computation:

When A is HIGH, Q_0 is saturated and F will be LOW.
With $V_{CE(sat)} = 0.2V$ all the load gates will be in the OFF state.

When A is LOW, Q_0 will be OFF and F will be at HIGH level.
Now it is required that the voltage at F is sufficient to ensure all the load gates Q_1 to Q_n saturated. Each load gate added to F will require a certain base current to cause saturation of the load transistor.

Note, $I_{C(EOS)} = (V_{CC} - V_{CE(sat)})/R_C$ and $I_{B(EOS)} = I_{C(EOS)}/\beta_F$

Now for one load gate, the base current for the load transistor $I_B = (V_{CC} - V_{BE(sat)})/(R_C + R_B)$

For two load gate, $I_{B2} = (V_{CC} - V_{BE(sat)})/(R_C + R_B/2)$

For total N load gate, $I_{BT} = (V_{CC} - V_{BE(sat)})/(R_C + R_B/N)$

For a maximum fanout of N, $I_{BT} \geq N\, I_{B(EOS)}$

Therefore $(V_{CC} - V_{BE(sat)})/(R_C + R_B/N) \geq N(V_{CC} - V_{CE(sat)})/(R_C\, \beta_F)$

Substituting, $N \leq 50\ (5\text{-}0.7)/(5\text{-}0.2) - (10/1) = 34.9$ Rounding down N = 34

Alternate Calculation:

A limit in the fanout is set when the voltage at F is insufficient to cause the transistor of the load gate to saturate. Note that $V_{IH} = 1.66V$

Then $I_{BT} = (V_{CC} – V_F)/R_C = (5 – 1.66)/1 = 3.34$ mA

$I_B = (V_F – V_{BE(sat)})/R_B = (1.66 – 0.7)/10 = 0.096$ mA

$N = I_{BT}/I_B = 34.79 \rightarrow 34$

Effect of Noise Margin on Fanout

Inclusion of Noise Margin reduces the fanout in the following manner

For a 0.5V noise margin

Minimum HIGH level voltage at F

$V_{OH} = V_{IH} + NM_H = 1.66 + 0.5 = 2.16V$

With V_F at 2.16V there remains an in-built safety margin at the input of load gates.

Similar calculation as above gives

$I_{BT} = (V_{CC} – V_F)/R_C = (5 – 2.16)/1 = 2.84$ mA

$I_B = (V_F – V_{BE(sat)})/R_B = (2.16 – 0.7)/10 = 0.15$ mA

$N = I_{BT}/I_B = 19.4 \rightarrow 19$

An increased NM_H reduces fanout even further.

The Base Overdrive Factor (k)

This is the ratio of actual base current and the base current required to just saturate the transistor. This is to account for transistor parameter variation like β_F.

For $V_{BE(sat)} = 0.7V$, $V_{CE(sat)} = 0.2V$, $\beta_F = 50$, $R_C = 1K\Omega$, $R_B = 10K\Omega$, 10 load gates

$I_{B(EOS)} = I_{C(EOS)}/\beta_F = (5\text{-}0.2)/(1x50) = 0.096mA$, $I_{BT} = (V_{CC} – V_{BE(sat)})/(R_C + R_B/10)$

$I_{BT} = (5\text{-}0.7)(1+10/10) = 2.15mA$ $I_B = I_{BT}/10 = 0.215mA$ Hence, $k = 0.215/0.096 = 2.24$

Worst-case Design

Here, circuit is analyzed by using the particular combination of parameter values which will result in an extreme value of the desired variable.

Analysis for fanout including overdrive factor k :

$$N \le \frac{\beta_F}{k} \cdot \frac{V_{CC} - V_{BE(sat)}}{V_{CC} - V_{CE(sat)}} - \frac{R_B}{R_C}$$

For worst case analysis, to choose extreme values of the variables in RHS that minimizes fanout.

$$N \le \frac{\underline{\beta_F}}{k} \cdot \frac{\underline{V_{CC}} - \cancel{V_{BE(sat)}}}{\cancel{V_{CC}} - \underline{V_{CE(sat)}}} - \frac{\cancel{R_B}}{\underline{R_C}}$$

Then underlined variables are to be at maximum and those have double strikethrough are to be at minimum. Since V_{CC} falls under both we have to check both the cases. Also R_B and R_C generally increase or decrease together in same percentage terms.

If $4.5 < V_{CC} < 5.5$, $0 < V_{CE(sat)} < 0.5$, $20 < \beta_F < 100$, $0 < V_{BE(sat)} < 0.5$, $k = 1$

With V_{CC} at minimum,

$$N \le \frac{20}{1} \cdot \frac{4.5 - 1}{4.5 - 0} - \frac{10}{1} \qquad \text{or } N \le 5.5$$

With V_{CC} at maximum,

$$N \le \frac{20}{1} \cdot \frac{5.5 - 1}{5.5 - 0} - \frac{10}{1} \qquad \text{or } N \le 6.4$$

Therefore in worst case situation fanout is 5.

Resistor Transistor Logic

This was among first commercially available digital IC s introduced by Fairchild in 1961.

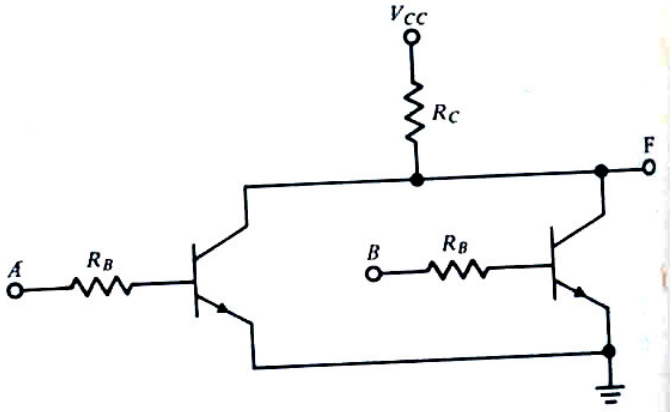


FIGURE 3.5
Circuit diagram of an RTL gate.

Motorola MC824AP, Quad 2 input NOR gate

V_{CC} = 3.6V, R_B = 450Ω, R_C = 640Ω,

V_{in} vs. V_{out} curve for MC824AP RTL gate(n=1 and n=5)
Vertical scale 0.5V/division, Horizontal scale 0.2V/division

We see $V_{OL} \approx 0.15V$, $V_{IL} \approx 0.6V$, HIGH output is function of number of load gates.

For 5 load gates, logic swing = $V_{OH} - V_{OL} = 1.15 - 0.15 = 1.0V$

$$NM_L = V_{IL} - V_{OL} = 0.6 - 0.15 = 0.45V$$

$$NM_H = V_{OH} - V_{IH} = 1.15 - 0.70 = 0.45V$$

Power Dissipation

With all 4 inputs at HIGH level, $PD_H = 4 \times 25 = 100$ mW

With all 4 inputs at LOW level, $PD_L = 4 \times 7.5 = 30$ mW

Average power dissipation is calculated assuming inputs spend as much time in HIGH state as in LOW state

PD_{av} per gate = (25 + 7.5)/2 = 16mW

Propagation Delay

Due to circuit capacitances and the finite switching speed of transistors, there is a delay from the time a signal is applied to the input of a logic gate until the desired change appears at the output of a gate.

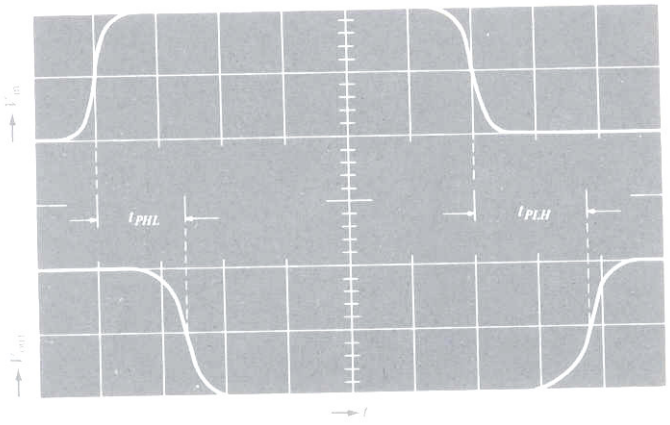


FIGURE 3.8
Waveforms showing effect of propagation delay time. Horizontal scale: 10 ns/cm.

V_{in} on top and V_{out} at bottom. Horizontal scale 10ns/division

Turn on delay = t_{PHL} : Delay in output changing from HIGH to LOW

Turn off delay = t_{PLH} : Delay in output changing from LOW to HIGH

Propagation delay t_{PD} is average of turn on and turn off delay. Here $t_{PD} \approx 12$ns

Figure of Merit

It is sometimes possible to decrease the propagation delay time by increasing operating current of transistors in the circuit. But that increases power consumption. The product

$$F = t_{PD} \times PD$$

serves as useful figure of merit on performance of a gate. The lower it is the better. For this gate

$$F = (12ns)(16mW) = 192pJ.$$

In low power RTL gate with $V_{CC} = 3.6V$, $R_B = 1.5K\Omega$, $R_C = 3.6K\Omega$, $t_{PD} = 27ns$ but the power dissipation with the inputs HIGH is 5mW per gate.

Direct-coupled Transistor Logic

One method of reducing propagation delay time is to eliminate base resistor and make a direct connection from the collector of a driving transistor to the base of load transistor.

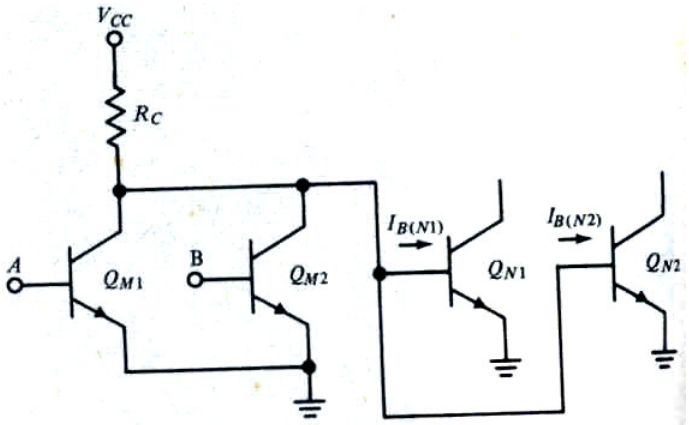
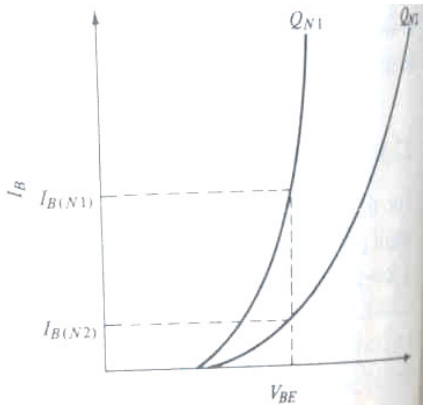


FIGURE 3.9
Circuit diagram of DCTL gates.

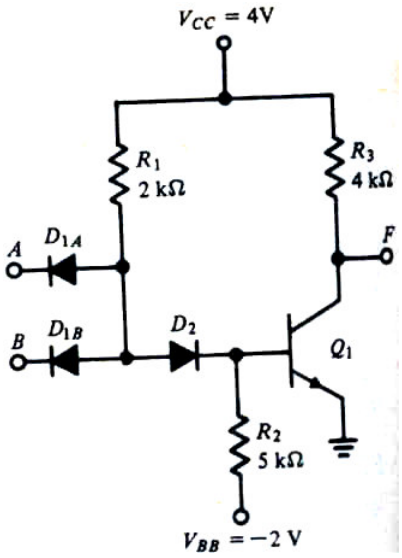


The circuit though simple has a severe limitation like input characteristics of all the load transistors should be well matched under all conditions. Else one of them will try to take the most of the current available in the form of current-hogging. This might lead to any of other load transistors out of saturation.

The defect can be diminished by placing a resistor in series with the base. Then the base current is less dependent on V_{BE} characteristic of the transistor. But that is typical RTL circuit.

Diode-Transistor Logic (DTL)

The disadvantage of RTL gate is small logic swing (≈ 1V) and hence lower noise margin.
A simple DTL circuit is a diode AND gate followed by an inverter giving NAND output.



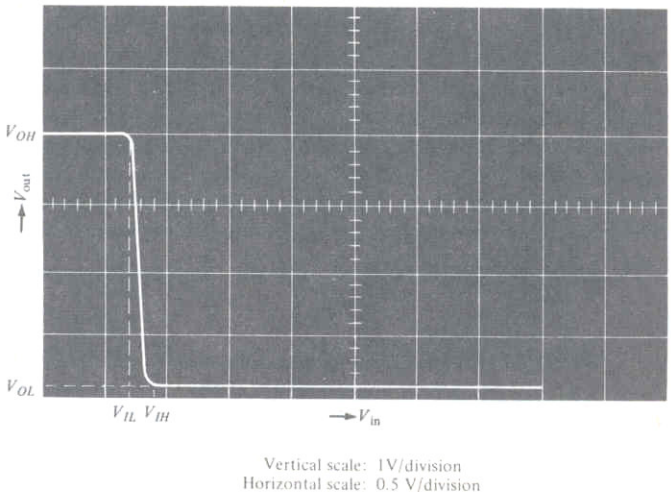


FIGURE 3.12
Voltage transfer characteristic of DTL gate.

LOW level output is represented by $V_{CE(sat)}$. At the LOW level threshold the input voltage must be sufficiently positive to turn off the input diodes and start turning on the output transistor.

$V_{IL} = V_{BE(sat)} + V_{D2(on)} - V_{D1(on)} = V_{BE(sat)} = 0.7V$ and $NM_L = V_{IL} - V_{OL} = 0.7 - 0.2 = 0.5V$

LOW level noise margin can be increased by placing two diodes in series instead of D_2. Then

$V_{IL} = V_{BE(sat)} + 2V_{D2(on)} - V_{D1(on)} = V_{BE(sat)} + V_{D2(on)} = 0.7 + 0.7 = 1.4V$

and $NM_L = V_{IL} - V_{OL} = 1.4 - 0.2 = 1.2V$

HIGH level output is represented by V_{CC} (= V_{OH}). Then input diodes of load gates are reverse biased and draws negligible reverse current. And there is no current hogging problem. The base current to transistor of a particular stage is decided by its own base resistance (R_1).

$NM_H = V_{OH} - V_{IH} = 4.0 - 0.9 = 3.1V$

Logic swing = $V_{OH} - V_{OL} = 4 - 0.2 = 3.8V$

Transition width = $V_{IH} - V_{IL} = 0.9 - 0.7 = 0.2V$

The output of RTL acts like current source while for DTL it acts like current sink.

Fanout of Basic DTL gate

A basic DTL circuit with two voltage offset diodes is shown.

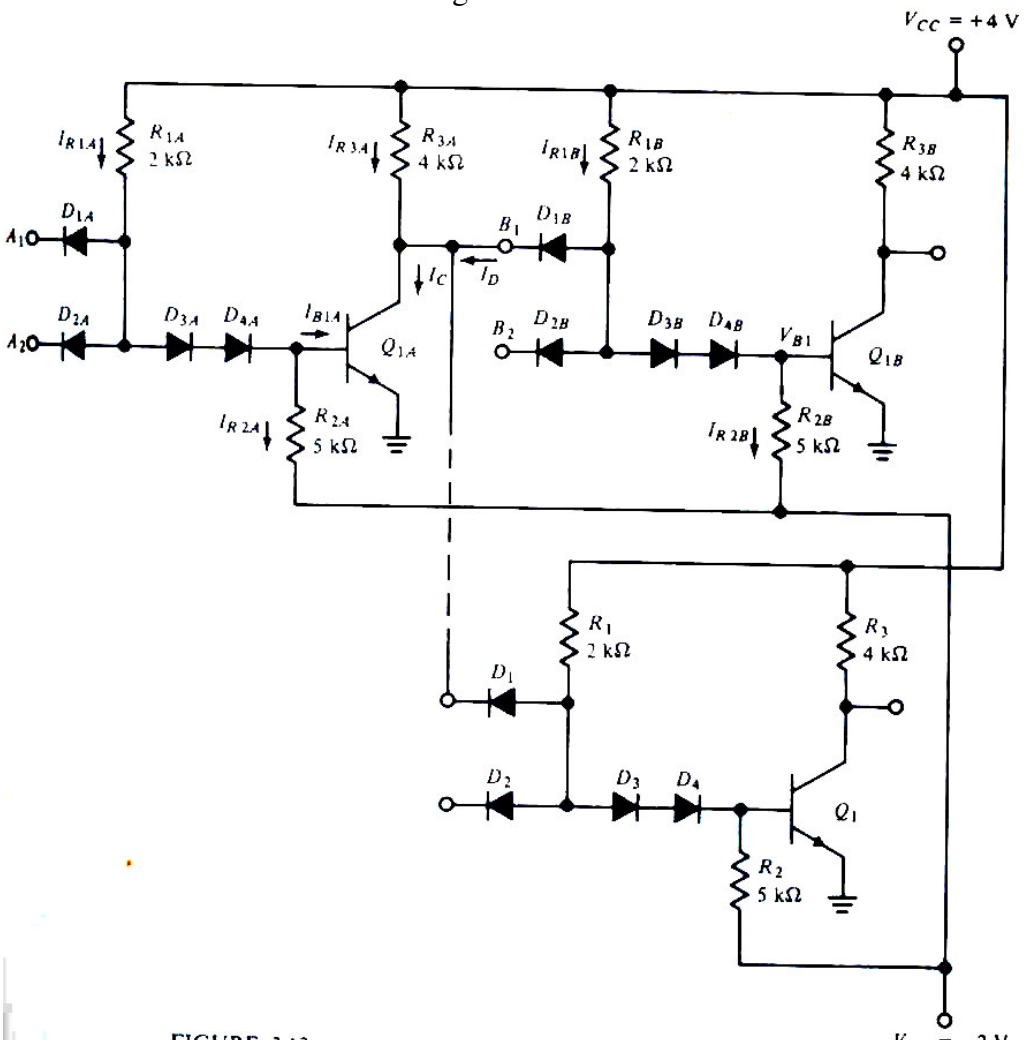


FIGURE 3.13
The basic DTL gate (whose output is at the collector of Q_{1A}) loaded with n other gate inputs.

From the figure, fanout = $((I_C - I_{R3A})/I_D$.

For $V_{BE(sat)} = V_{D(on)} = 0.7V$, $\beta_F = 20$, $V_{CE(sat)} = 0.2V$, k = 1

$I_{R1A} = (V_{CC} - 2V_{D(on)} - V_{BE(on)})/R_{1A} = (4 - 1.4 - 0.7)/2 = 0.95mA$

$I_{R2A} = (V_{BE(on)} - V_{BB})/R_{2A} = (0.7 + 2)/5 = 0.54mA$ $I_{B1A} = 0.95 - 0.54 = 0.41mA$

The collector current at the edge of saturation $I_C = 20 \times 0.41 = 8.2mA$

$I_{R3A} = (V_{CC} - V_{CE(sat)})/R_{3A} = (4 - 0.2)/4 = 0.95mA$

At the output gate transistor base

$V_{B1} = V_{CE(sat)} + V_{D(on)} - 2V_{D(on)} = V_{CE(sat)} - V_{D(on)} = 0.2 - 0.7 = -0.5V$

These transistors are cut off.

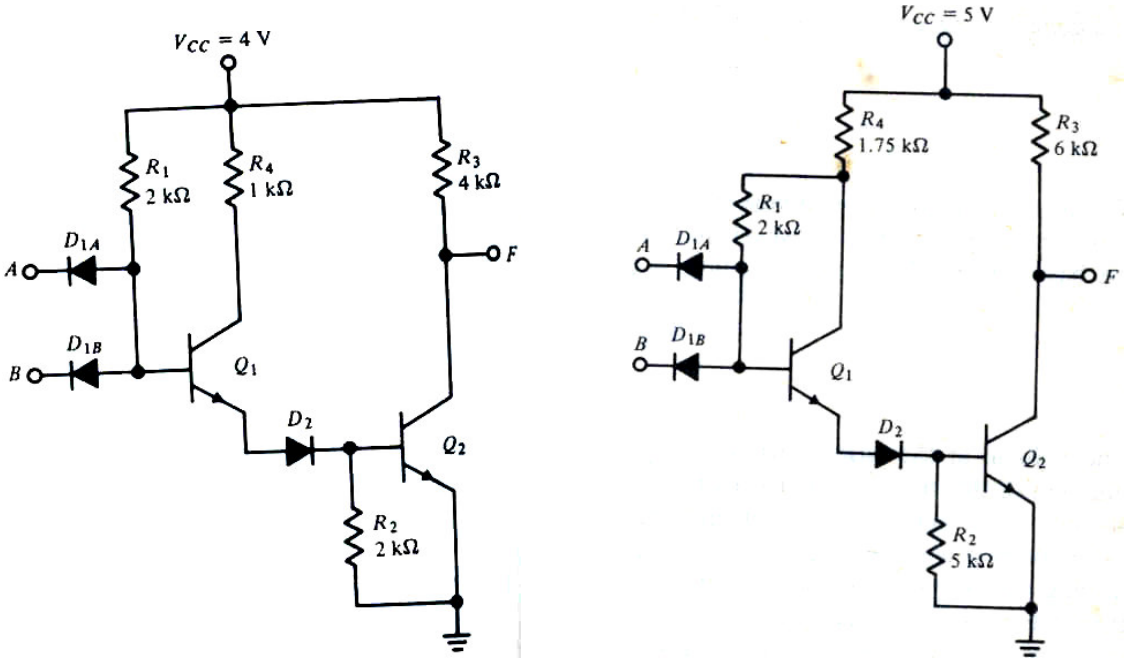
$I_{R1B} = (V_{CC} - V_{CE(sat)} - V_{D(on)})/R_{1B} = (4 - 0.2 - 0.7)/2 = 1.55mA$

$I_{R2B} = (V_{B1} - V_{BB})/R_{2B} = (-0.5 + 2)/5 = 0.3mA \quad I_D = 1.55 - 0.3 = 1.25mA$

Then, fanout $N = (8.2 - 0.95)/1.25 = 5.8 \rightarrow 5$

Note that this is not worst case fanout.

Modified DTL Gate



The first circuit shows removal one level shifting diode by one emitter follower. This increases base current to Q_2 increasing fanout.. R_4 prevents Q_2 going deep in saturation if less load is connected. But then Q_1 also saturates.

The feedback biasing second circuit (through R_1) prevents Q_1 from saturating. As collector current increases, collector voltage falls and base current too falls.

Fanout calculation

$V_{CC} - 3V_{BE(on)} = I_{B1}(R_1 + R_4) + I_{C1} R_4$ and $I_{C1} = \beta_F I_{B1}$ since Q_1 is not saturated.

Base current of Q_1 : $I_{B1} = \dfrac{V_{CC} - 3V_{BE(on)}}{(R_1 + R_4) + \beta_F R_4} = (5 - 2.1)/(3.75 + 20x1.75) = 0.075mA$

$I_{C1} = \beta_F I_{B1} = 20x0.075 = 1.5mA$

Note, $V_{C1} = V_{CC} - R_4(I_C + I_B) = 5 - 1.75x1.575 = 2.25V$, $V_{B1} = 2.1V$. So BC is reverse biased and hence in active region.

Now $I_{E1} = 0.075 + 1.5 = 1.58mA$ and $I_{B2} = I_{E1} - V_{B2}/R_2 = 1.58 - 0.7/5 = 1.44mA$

The collector current of Q_2 at the edge of saturation $I_{C2} = \beta_F I_{B2} = 20x1.44 = 28.8mA$

$I_{R3} = (V_{CC} - V_{CE(sat)})/R_3 = (5 - 0.2)/6 = 0.8mA$

For the load gates input is LOW

So $V_{B1(L)} = V_{CE(sat)} + V_{D(on)} = 0.2 + 0.7 = 0.9V$

This voltage is insufficient to turn on Q_1 thorough D_2.

Then $I_D = (V_{CC} - V_{CE(sat)} - V_{D(on)})/(R_1 + R_4) = (5 - 0.2 - 0.7)/3.75 = 1.09mA$

Then, fanout $N = (28.8 - 0.8)/1.09 = 25.6 \rightarrow 25$

Note, in high threshold DTL, D_2 is replaced with zener diode of 6 V, V_{CC} is 15V and to avoid excessive power dissipation the values of resistors are increased.

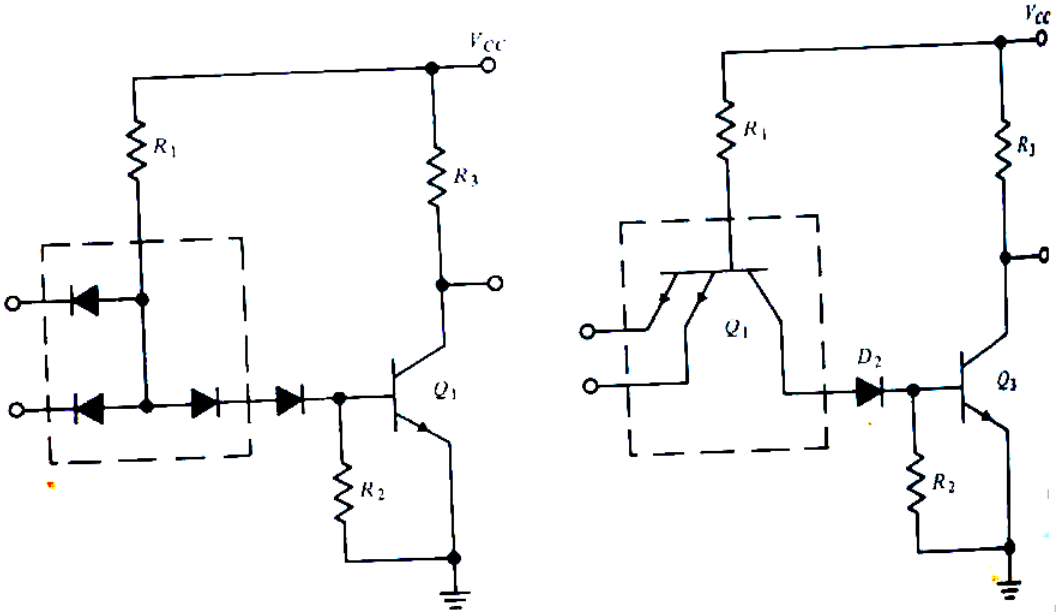
MC930 dual expandable 4 input gate with following specification:

$V_{OH} = 2.6V$, $V_{OL} = 0.4V$, $V_{IL} = 1.1V$, $V_{IH} = 2.0V$, $P_{DH} = 11.9mW$, $P_{DL} = 5.45mW$, $F = 285pJ$

RTL thus is faster. But fanout, logic swing, noise margin are greater.

Transistor-Transistor Logic (TTL)

The fact that the characteristics of BE junction of a transistor is similar to a diode is used to advantage in TTL logic circuit. The input diodes of a DTL gate are replaced by a multi emitter transistor. The CB junction provides an offset voltage like an offset diode. The advantages are: (1) Silicon area saved (2) Improvement of switching speed (turning off of Q_3).



With input LOW ($V_{CE(sat)}$) :

BE junction of Q_1 is forward biased. But I_C for Q_1 is only leakage current of D_2 which is very small ($<< \beta_F I_B$) and hence Q_1 is in saturation. So voltage at collector of Q_1 is nearly 0.2V higher than the emitter voltage. So insufficient voltage to forward bias D_2 and subsequently Q_3. Q_3 is off. Output is held at V_{CC}, HIGH logic level.

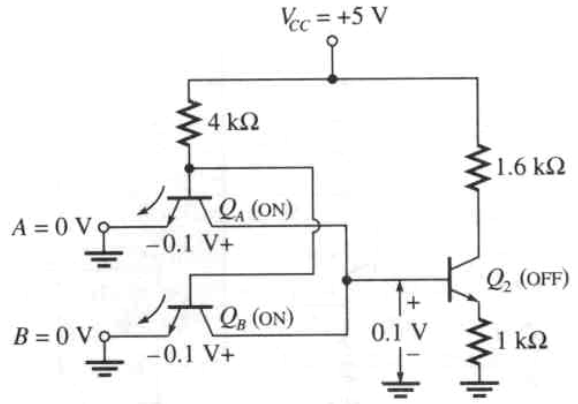
With all inputs at HIGH (V_{CC}) :

BE junction of Q_1 is reverse biased. Current flows from V_{CC} through R_1, forward biased BC junction of Q_1, D_2 into BE junction of Q_3. This current is sufficient to saturate Q_3 resulting LOW logic level at the output of the gate.

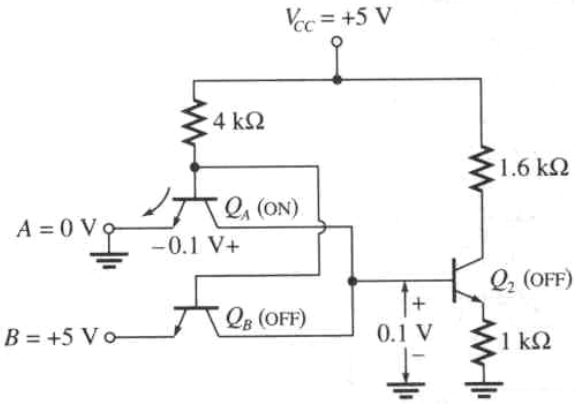
Note that the input transistor now works in the inverse mode with E and C changing their roles. With emitter acting as collector

$I_{E1} = \beta_R I_{B1} = \beta_R I_B/M$ where M = Total no. of emitters in Q_1 and I_B = Total base current

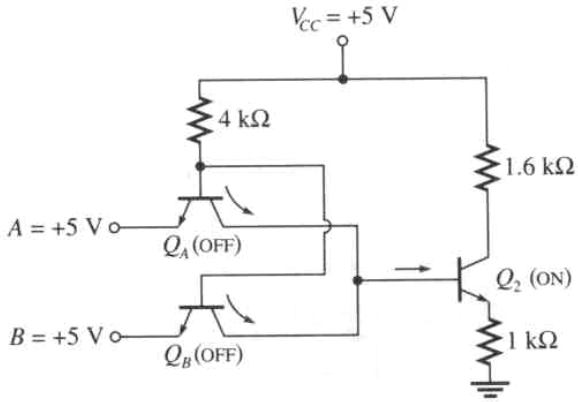
$I_{C1} = (\beta_R + 1)I_{B1} + (\beta_R + 1)I_{B2} + \ldots = (\beta_R + 1)I_B$



(a) When inputs A and B are both 0 V, Q_A and Q_B are both ON, so Q_2 is OFF.



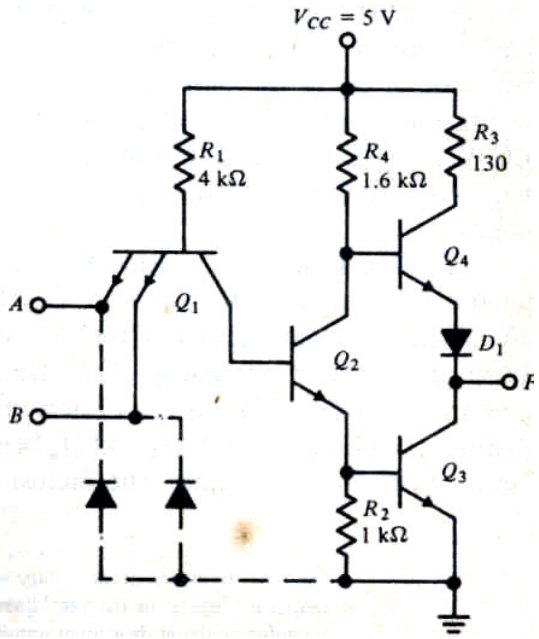
(b) When input A (or input B) is 0 V, Q_A (or Q_B) is ON, so Q_2 is OFF.



(c) When inputs A and B are both +5 V, Q_A and Q_B are both OFF. Current flows from base to collector in Q_A and Q_B, supplying base current to turn on Q_2.

Modification

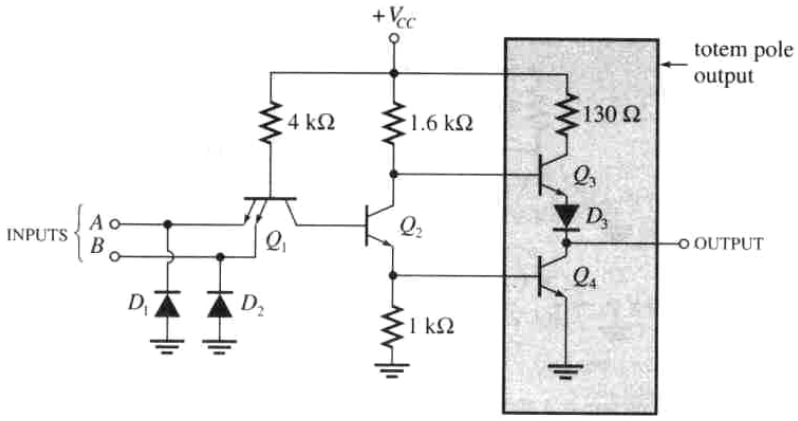
The previous circuit gives problem if β_R is high, then a large amount of current flows to input. This current with collector load resistance can bring down HIGH level voltage considerably. A *totem-pole* output reduces output resistance for both HIGH & LOW output.



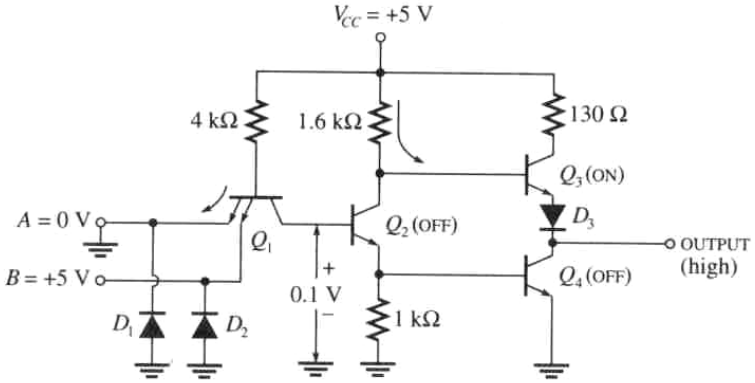
Note that for all logic families like RTL, DTL, modified DTL for LOW level output resistance is nearly 10 ohm while for HIGH level it is 650-6000 ohm. With totem-pole TTL gives output resistance of less than 100 ohm for HIGH level output. This also quickens charging/discharging of capacitance at the gate output.

Q_2 besides serving as level shifter similar to D_2 acts as *phase splitter*. Voltage at C & E of Q_2 are 180 degree out of phase. Thus when there is LOW at E of Q_2 to turn off Q_3 there is HIGH at C of Q_2 to turn on Q_4 and *vice versa*.

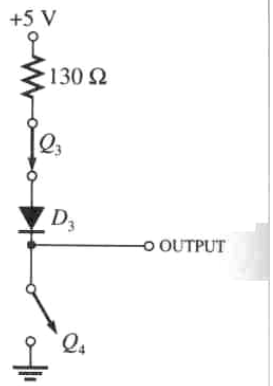
The diode D_1 is required to avoid an indeterminate output level. With LOW level at output both Q_2 and Q_3 are saturated. Their collector voltages w.r.t. ground are 0.9V and 0.2V respectively. The voltage 0.9V in absence of D_1 turns on Q_4. Then current will be diverted from collector of Q_2 to base of Q_4 and thus Q_2 will come out of saturation. Then both Q_3 and Q_4 will be conducting resulting in indeterminate output level.



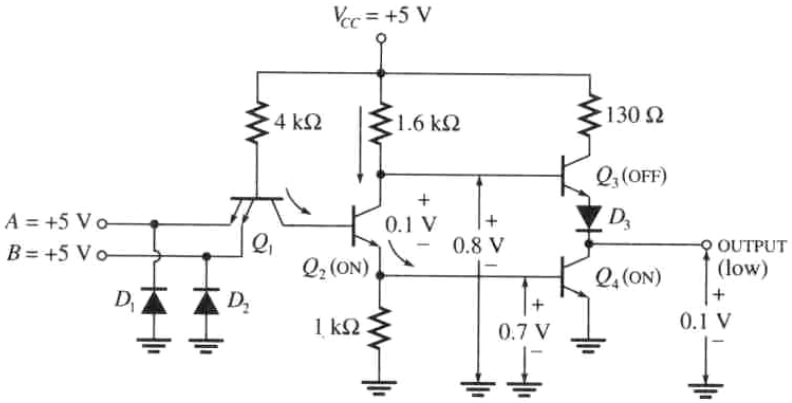
(a) A totem pole output connected to the multiple-emitter input.



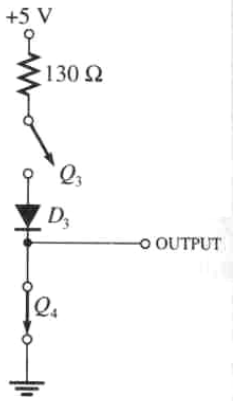
(b) Static analysis when Q_2 is off.



(c) Totem pole equivalent.



(d) Static analysis when Q_2 is on.



(e) Totem pole equivalent.

Figure 10.4
Static analysis of one gate in a 7400 quad 2-input NAND *gate, including the totem pole output.*

Why not $R_3 = 0$?

With input HIGH, Q_3 in saturation and output LOW.
Now input going LOW, Q_2 turns off, its collector rises turning on Q_3. If Q_3 is slow to come out of saturation both the transistors are on briefly and high current may result. During this switching

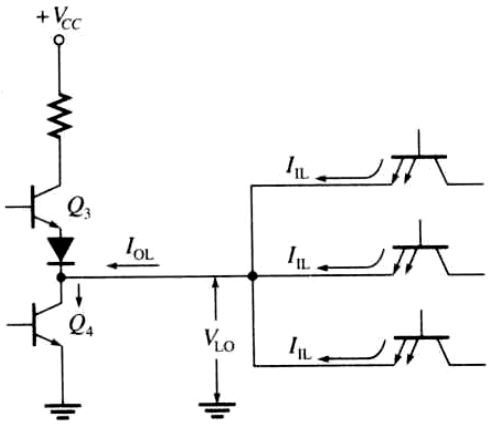
$$I = (V_{CC} - (V_{CE3(sat)} + V_{D1(on)} + V_{CE4(sat)}))/R_3 = 30 \text{ mA (comes as spike in power supply)}$$

Note this also protects when logic HIGH output is accidentally grounded to limit the current.

Fanout of TTL Gate

With output LOW:

Figure 10.7
A TTL output driving several TTL loads. I_{OL} is the sum of the currents supplied by the loads and Q_4 must be capable of sinking all of this current.



<u>To consider how much current Q_3 can sink first.</u> Note that Q_2 and Q_3 both are in saturation.

Now at Q_1, $V_{B1} = 2V_{BE(sat)} + V_{BC(sat)} = 2x0.7 + 0.5 = 1.9V$ $[V_{BC(sat)} = 0.5V]$

Then $I_{B1} = (V_{CC} - V_{B1})/R_1 = (5 - 1.9)/4 = 0.78mA$

Then $I_{C2} = (V_{CC} - V_{CE(sat)} - V_{BE(sat)})/R_4 = (5 - 0.2 - 0.7)/1.6 = 2.56mA$

Note that, $I_{B2} = I_{C1} = (\beta_R+1)I_{B2}$

If $\beta_R = 0.2$ then $\beta_F = I_{C2}/[(\beta_R+1)I_{B2}] = 2.56/(1.2x0.78) = 2.8$ is sufficient to saturate Q_2.

Again, $I_{B3} = I_{B2} + I_{C2} - V_{BE(sat)}/R_2 = 0.93 + 2.56 - 0.6/1 = 2.79mA$

At the EOS for Q_3, $I_{C3} = \beta_F I_{B3} = 20x2.79 = 55.8mA$ (Typical value of $\beta_F = 20\text{-}100$)

To consider how much is the load current next.

$I_{E1} = (V_{CC} - V_{CE(sat)} - V_{BE(sat)})/R_1 = (5 - 0.2 - 0.7)/4 = 1.02mA$ [Since, β_R is small.]

So $N_L = I_{C3}/I_E = 55.8/1.02 \rightarrow 54$

With output HIGH :

Let us calculate the fanout possible if output HIGH voltage level becomes 2.4V due to loading effect.

With Q_4 conducting, voltage at base of $Q_4 = 2x0.7 + 2.4 = 3.8V$

Then Q_2 is cut off and voltage drop across R_4 is due to base current of Q_4.

$I_{B4} = (5 - 3.8)/1.6 = 0.75mA$ and $I_{C4} = (5 - 0.2 - 0.7 - 2.4)/0.13 = 13.1mA$

$I_{E4} = I_{B4} + I_{C4} = 13.85mA$

The base current of the load transistor Q_1 is determined as 0.78mA. It acts in inverse mode. With $\beta_R = 0.2$ input current to load gate = 0.2x0.78 =0.156mA

Then $N_H = 13.8/0.156 \rightarrow 88$ (= 176 if two emitter)

[Note, $N_H > N_L$ is common to TTL gate circuits.]

54 series TTL

Recommended $V_{CC} = 5.0V \pm 10$ percent ; Operating Temperature –55 to +125 degree centigrade

Fanout = 10, $V_{OH} = 3.1V$, $V_{OL} = 0.2V$, $V_{IL} = 1.2V$, $V_{IH} = 1.4V$

Short circuit output current = 34mA

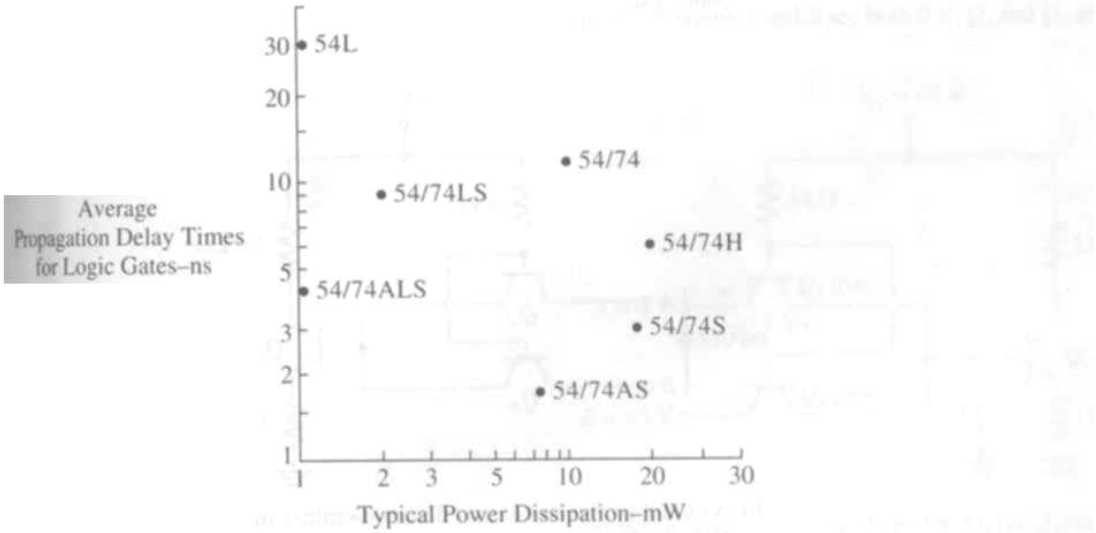
[$I_{C4(sat)}$ with output at 0V = (5 – 0.2 – 0.7 – 0)/0.13 = 31.6mA and $I_{B4} = (5 - 1.4)/1.6 = 2.2mA$]

V_{CC} supply current per gate when output LOW, no load(sum of I_{C2} and I_{B2}) = 3.6mA

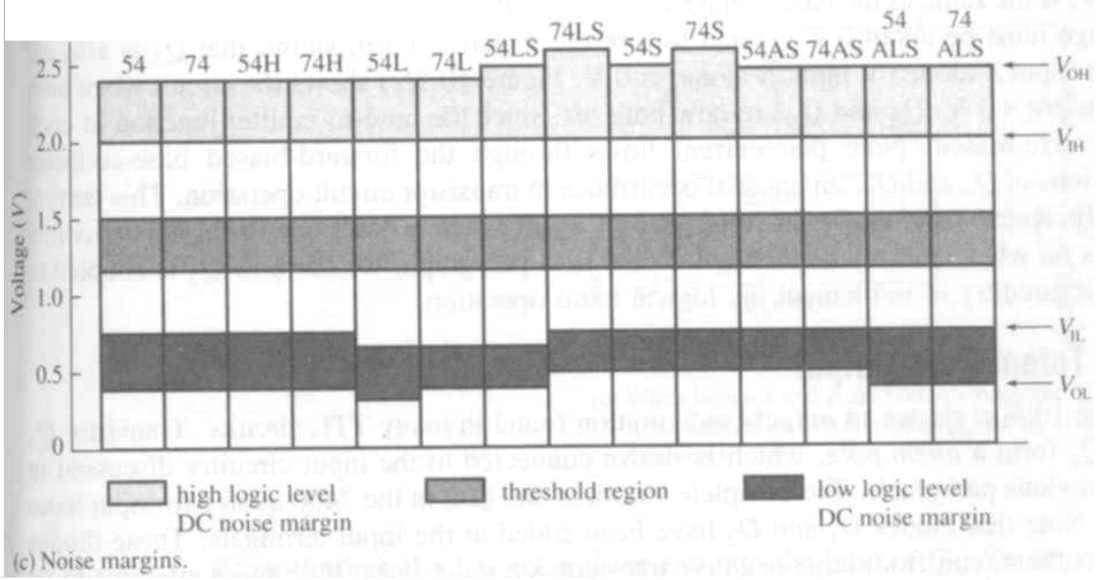
V_{CC} supply current per gate when output HIGH, no load ($I_{B1} = I_{E1}$) = 1.1mA

Power dissipation = $V_{CC} (I_{CCL} + I_{CCH})/2 = 10mW$

Typical propagation delay, $t_{pd} = 9ns$ Figure of merit = 9x10 = 90pJ



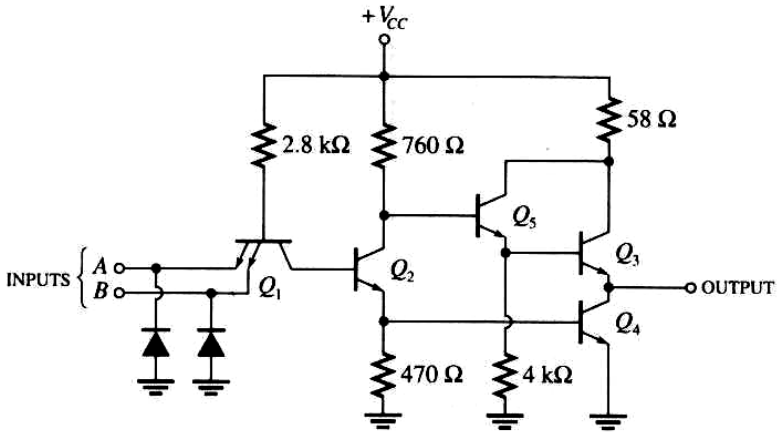
(b) Speed-power relationships.



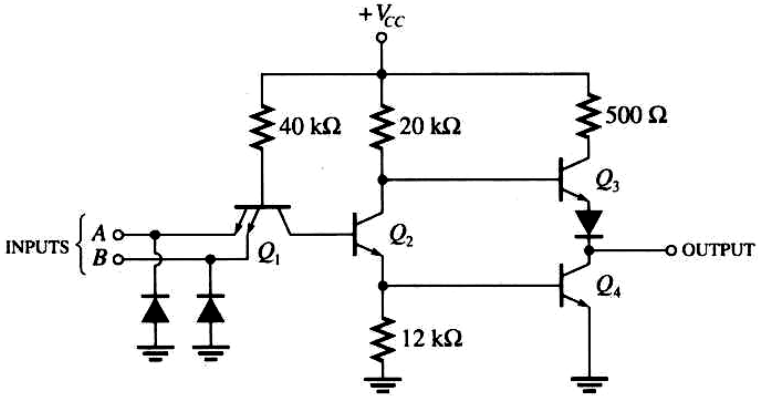
(c) Noise margins.

High Speed (H) and Low Power (L) TTL

In High Speed TTL, lower resistance values are used with an additional pull up transistor Q_5 in the form of *Darlington pair* which has much greater current gain. The diode in the totempole output no longer needed.



(a) 74H00 NAND gate.



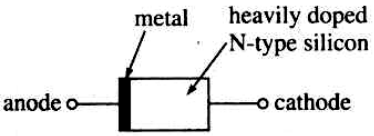
(b) 74L00 NAND gate.

Figure 10.8
Typical high-speed (H) and low-power (L) TTL gates.

For low power TTL, larger resistance values are used, which reduces power consumption at the expense of speed.

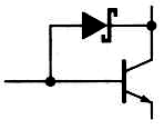
Schottky (S) and Low Power Schottky (LS) TTL

This is to prevent transistor going deep into saturation by clamping BC forward bias voltage. This reduces *storage time delay* as excess charge carriers are prevented at the junction. A clamp of less than 0.7V is required. Though Ge diode can provide that but it is difficult to fabricate it on Si chips. Schottky diode having metal-semiconductor junction with forward drop of 0.3-0.4V is used.



(a) Schottky diode construction.

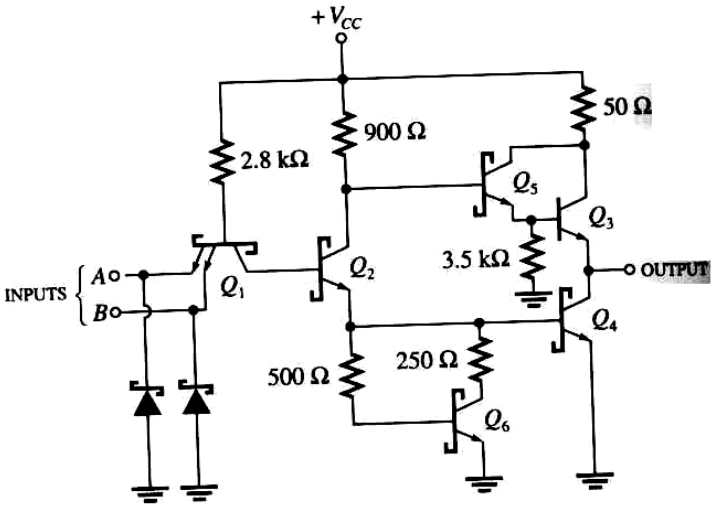
(b) Schottky diode symbol.



(c) A Schottky-clamped NPN transistor.

(d) Equivalent symbol for (*c*).

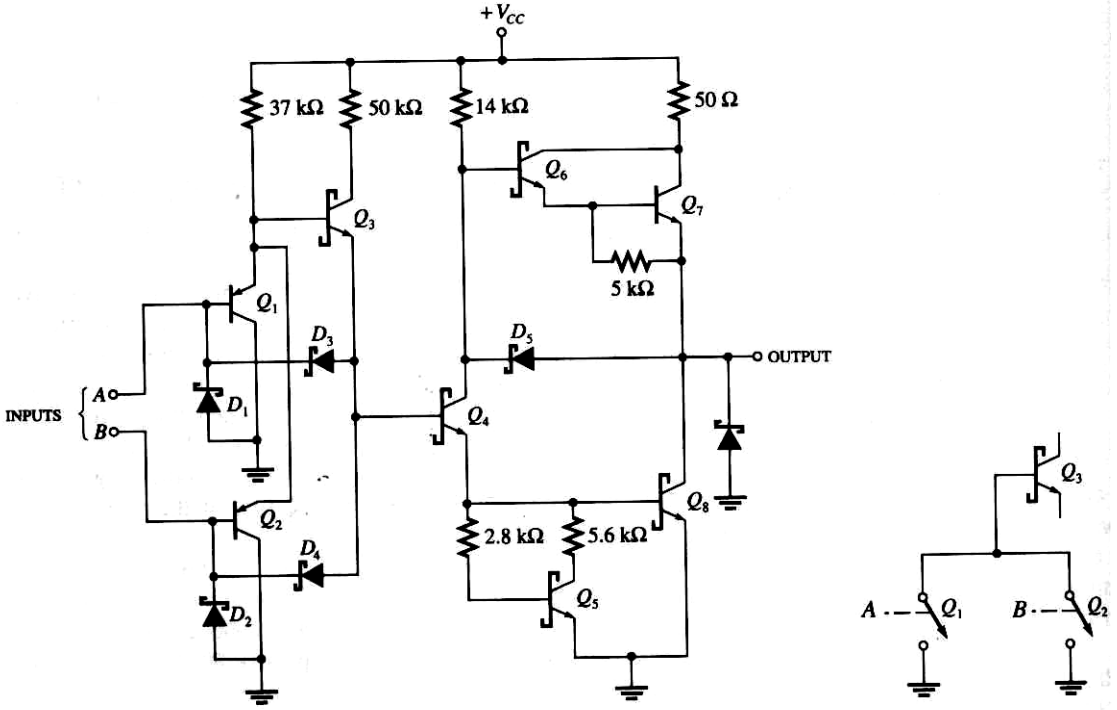
Figure 10.9
The Schottky diode and Schottky clamp.



(a) One gate in the 74S00 quad two-input NAND gate.

Advanced Schottky (AS) and Advanced Low Power Schottky (ALS) TTL

ALS and AS technologies are recent enhancements in the form of doping technique (ion implantation instead of diffusion), improved isolation (reduces capacitance and improves switching time), and addition of more complex circuitry to have higher speed, lower power consumption and increased fanout.



(a) One gate in the 74ALS00A quad 2-input NAND gate.

(b) Equivalent input switching circuit.

Figure 10.13
Typical advanced Schottky (AS) and advanced low-power Schottky (ALS) gates.

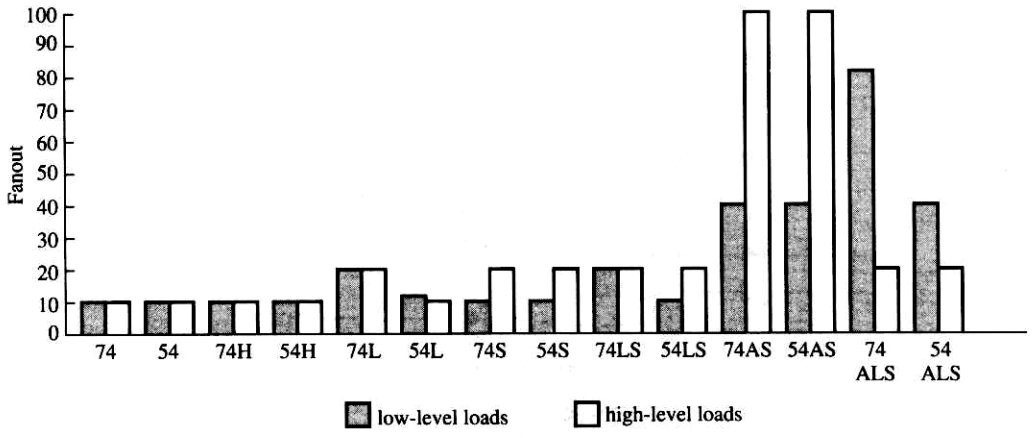
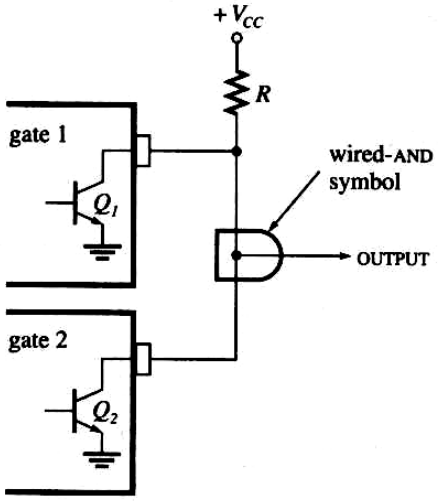


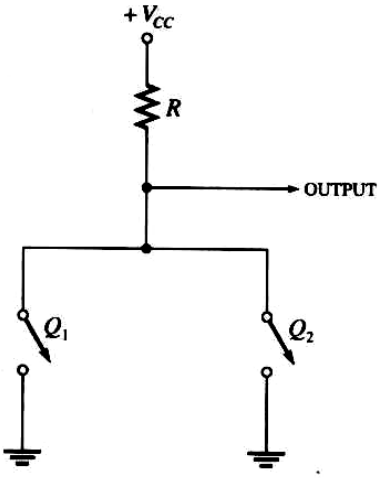
Figure 10.12
Comparison of fanouts for TTL subfamilies.

Open-Collector outputs – Wired AND

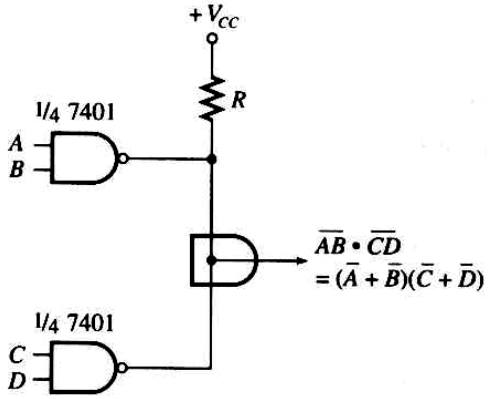
The output of such gates are simply the collector of the pull-down transistor, which the user may connect to an external resistor and power-supply voltage. LED, relay coils can be connected at the output also it can be used to logically AND the outputs of the gates. The resistance is also called pull up resistor.



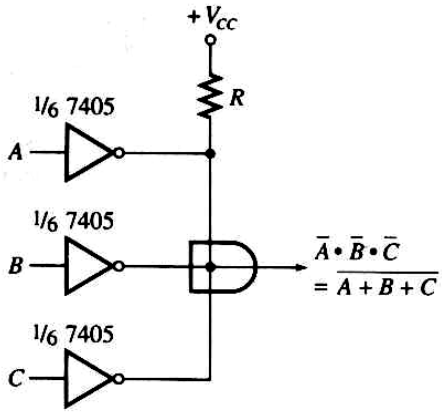
(a) Connecting open-collector outputs to perform a wired-AND operation. Each transistor is off if the output of its respective gate is high (logical 1)



(b) Switching equivalent of (*a*). The output is high only if Q_1 and Q_2 are both open; i.e., only if the outputs of gates 1 and 2 are both high.



(c) Wire-ANDed output of two NAND gates.

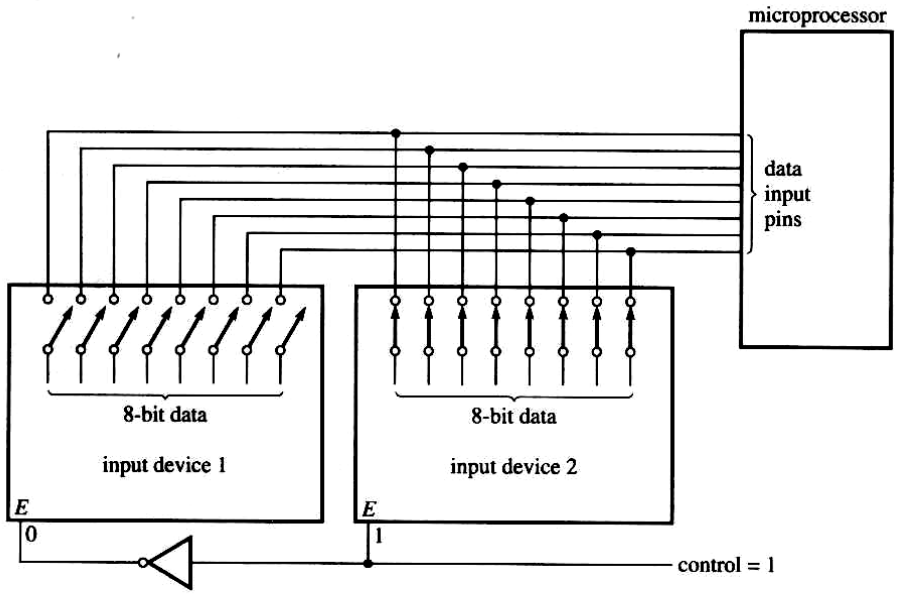


(d) The wire-ANDed output of inverters implements the NOR operation.

Absence of pull up transistor reduces switching speed. However the are useful in reducing *chip count* of a system where speed is not a consideration.

Three (Tri) State Logic

Tristae Logic is used to prevent HIGH output being short circuited with LOW output e.g. for bus drivers in sharing a bus.



(b) Input device 1 is effectively disconnected from the bus while input device 2 is connected to it. The open switches represent high-impedance states. When its *E* (enable) input is high, a device has *control* of the bus.

This has an addition Control input in the form of ENABLE. The circuit operates normally when enabled. Else the output goes into a high impedance state (third state) where it neither drives nor sinks current. IC 74AS231 is TTL 8 input bus driver.

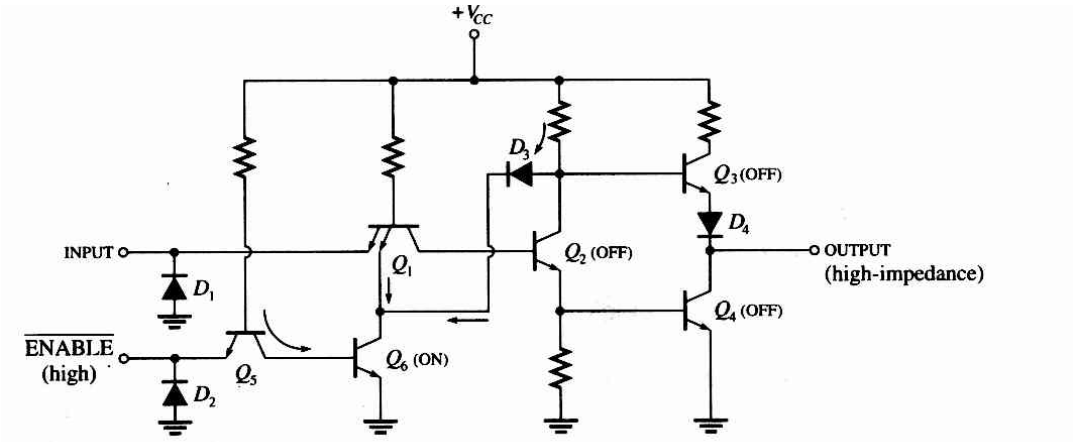


Figure 10.18
An example of a TTL inverter modified for three-state operation. The output is high impedance when $\overline{ENABLE}$ is high, the case illustrated here.